

TENTATIVE TOSHIBA MULTI-CHIP INTEGRATED CIRCUIT SILICON GATE CMOS

SRAM AND FLASH MEMORY MIXED MULTI-CHIP PACKAGE

DESCRIPTION

The TH50VSF2580/2581AASB is a mixed multi-chip package containing a 4,194,304-bit full CMOS SRAM and a 33,554,432-bit flash memory. The CIOS and CIOF inputs can be used to select the optimal memory configuration. The power supply for the TH50VSF2580/2581AASB can range from 2.7 V to 3.6 V. The TH50VSF2580/2581AASB can perform simultaneous read/write operations on its flash memory and is available in a 69-pin BGA package, making it suitable for a variety of applications.

FEATURES

- Power supply voltage
 $V_{CCs} = 2.7\text{ V} \sim 3.6\text{ V}$
 $V_{CCf} = 2.7\text{ V} \sim 3.6\text{ V}$
- Data retention supply voltage
 $V_{CCs} = 1.5\text{ V} \sim 3.6\text{ V}$
- Current consumption
 Operating: 45 mA maximum (CMOS level)
 Standby: 7 μA maximum (SRAM CMOS level)
 Standby: 10 μA maximum (flash CMOS level)
- Block erase architecture for flash memory
 8 blocks of 8 Kbytes
 63 blocks of 64 Kbytes
- Organization
 - Function mode control for flash memory
 Compatible with JEDEC-standard commands
 - Flash memory functions
 Simultaneous Read/Write operations
 Auto-Program
 Auto Chip Erase, Auto Block Erase
 Auto Multiple-Block Erase
 Program Suspend/Resume
 Block-Erase Suspend/Resume
 Data Polling / Toggle Bit function
 Block Protection / Boot Block Protection
 Support for automatic sleep and hidden ROM area
 Common flash memory interface (CFI)
 Byte/Word Modes
 - Erase and Program cycles for flash memory
 10^5 cycles (typical)
 - Boot block architecture for flash memory
 TH50VSF2580AASB: Top boot block
 TH50VSF2581AASB: Bottom boot block
- Package
 P-FBGA69-1209-0.80A3: 0.31 g (typ.)

| CIOF | CIOS | Flash Memory | SRAM |
|----------|----------|----------------------------|--------------------------|
| V_{CC} | V_{CC} | 2,097,152 words of 16 bits | 262,144 words of 16 bits |
| V_{CC} | V_{SS} | 2,097,152 words of 16 bits | 524,288 words of 8 bits |
| V_{SS} | V_{SS} | 4,194,304 words of 8 bits | 524,288 words of 8 bits |

PIN ASSIGNMENT (TOP VIEW)

- $CIOF = V_{CC}$, $CIOS = V_{CC} (\times 16, \times 16)$

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|----|-------------------|-----------------|-----------------|---------------------|-----------------|------|------|----------|----|
| A | NC | | | | | | | | | NC |
| B | NC | | | | | | | | | NC |
| C | NC | | A7 | \overline{LB} | $\overline{WP/ACC}$ | \overline{WE} | A8 | A11 | | |
| D | | A3 | A6 | \overline{UB} | \overline{RESET} | CE2S | A19 | A12 | A15 | |
| E | | A2 | A5 | A18 | $\overline{RY/BY}$ | A20 | A9 | A13 | NC | |
| F | NC | A1 | A4 | A17 | | | A10 | A14 | NC | NC |
| G | NC | A0 | V_{SS} | DQ1 | | | DQ6 | DU | A16 | NC |
| H | | \overline{CEF} | \overline{OE} | DQ9 | DQ3 | DQ4 | DQ13 | DQ15 | CIOF | |
| J | | $\overline{CE1S}$ | DQ0 | DQ10 | V_{CCf} | V_{CCs} | DQ12 | DQ7 | V_{SS} | |
| K | | | DQ8 | DQ2 | DQ11 | CIOS | DQ5 | DQ14 | | |
| L | NC | | | | | | | | | NC |
| M | NC | | | | | | | | | NC |

PIN NAMES

| | |
|---------------------------------------|--|
| A0~A21 | Address inputs |
| A12S | A12 input for SRAM |
| A12F | A12 input for flash memory |
| SA | A18 input for SRAM |
| DQ0~DQ15 | Data inputs/outputs |
| $\overline{CE1S}$, $\overline{CE2S}$ | Chip Enable inputs for SRAM |
| \overline{CEF} | Chip Enable input for flash memory |
| \overline{OE} | Output Enable input |
| \overline{WE} | Write Enable input |
| \overline{LB} , \overline{UB} | Data byte control input |
| $\overline{RY/BY}$ | Ready/Busy output |
| \overline{RESET} | Hardware reset input |
| $\overline{WP/ACC}$ | Write Protect / Program Acceleration input |
| CIOS | Word Enable input for SRAM |
| CIOF | Word Enable input for flash memory |
| V_{CCs} | Power supply for SRAM |
| V_{CCf} | Power supply for flash memory |
| V_{SS} | Ground |
| NC | Not connected |
| DU | Do not use |

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PIN ASSIGNMENT (TOP VIEW)

- CIOF = V_{CC}, CIOS = V_{SS} (×16, ×8)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|----|-------------------|-----------------|------|---------------------|------------------|------|------|-----------------|----|
| A | NC | | | | | | | | | NC |
| B | NC | | | | | | | | | NC |
| C | NC | | A7 | DU | $\overline{WP/ACC}$ | \overline{WE} | A8 | A11 | | |
| D | | A3 | A6 | DU | \overline{RESET} | CE2S | A19 | A12 | A15 | |
| E | | A2 | A5 | A18 | RY/BY | A20 | A9 | A13 | NC | |
| F | NC | A1 | A4 | A17 | | | A10 | A14 | NC | NC |
| G | NC | A0 | V _{SS} | DQ1 | | | DQ6 | SA | A16 | NC |
| H | | \overline{CEF} | \overline{OE} | DQ9 | DQ3 | DQ4 | DQ13 | DQ15 | CIOF | |
| J | | $\overline{CE1S}$ | DQ0 | DQ10 | V _{CCf} | V _{CCs} | DQ12 | DQ7 | V _{SS} | |
| K | | | DQ8 | DQ2 | DQ11 | CIOS | DQ5 | DQ14 | | |
| L | NC | | | | | | | | | NC |
| M | NC | | | | | | | | | NC |

- CIOF = V_{SS}, CIOS = V_{SS} (×8, ×8)

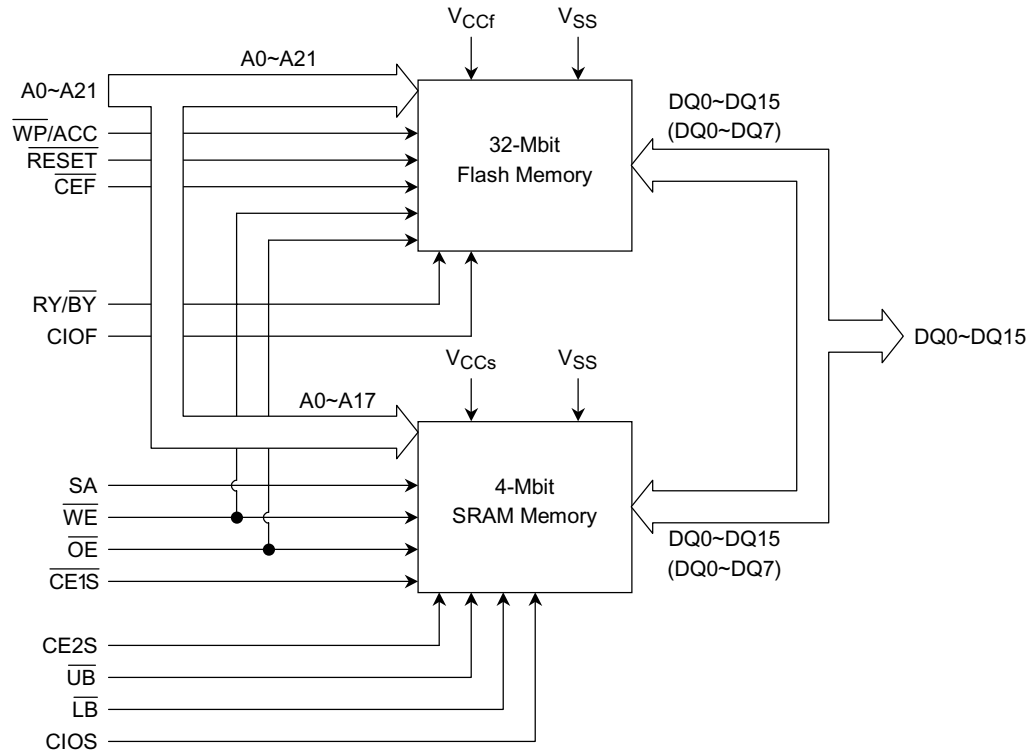
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|----|-------------------|-----------------|-----|---------------------|------------------|-----|------|-----------------|----|
| A | NC | | | | | | | | | NC |
| B | NC | | | | | | | | | NC |
| C | NC | | A7 | DU | $\overline{WP/ACC}$ | \overline{WE} | A8 | A11 | | |
| D | | A3 | A6 | DU | \overline{RESET} | CE2S | A20 | A13 | A16 | |
| E | | A2 | A5 | A19 | RY/BY | A21 | A9 | A14 | NC | |
| F | NC | A1 | A4 | A18 | | | A10 | A15 | NC | NC |
| G | NC | A0 | V _{SS} | DQ1 | | | DQ6 | A12S | A17 | NC |
| H | | \overline{CEF} | \overline{OE} | DU | DQ3 | DQ4 | DU | A12F | CIOF | |
| J | | $\overline{CE1S}$ | DQ0 | DU | V _{CCf} | V _{CCs} | DU | DQ7 | V _{SS} | |
| K | | | DU | DQ2 | DU | CIOS | DQ5 | DU | | |
| L | NC | | | | | | | | | NC |
| M | NC | | | | | | | | | NC |

Note: A12F and A12S should be wired together and used as a single A12 pin.

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BLOCK DIAGRAM



MODE SELECTION

| OPERATION MODE | $\overline{\text{CEF}}$ | $\overline{\text{CE1S}}$ | CE2S | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | $\overline{\text{RESET}}$ | $\overline{\text{UB}}$ | $\overline{\text{LB}}$ | $\overline{\text{WP/ACC}}$ | DQ0~DQ7 | DQ8~DQ15 |
|--------------------------------|-------------------------|--------------------------|---------------|------------------------|------------------------|---------------------------|------------------------|------------------------|----------------------------|------------------|------------------|
| Flash Read | L | H | X | L | H | H | X | X | X | D _{OUT} | D _{OUT} |
| | L | X | L | L | H | H | X | X | X | D _{OUT} | D _{OUT} |
| SRAM Read | H | L | H | L | H | H | L | L | X | D _{OUT} | D _{OUT} |
| | H | L | H | L | H | H | H | L | X | D _{OUT} | Hi-Z |
| | H | L | H | L | H | H | L | H | X | Hi-Z | D _{OUT} |
| Flash Write | L | H | X | H | L | H | X | X | X | D _{IN} | D _{IN} |
| | L | X | L | H | L | H | X | X | X | D _{IN} | D _{IN} |
| SRAM Write | H | L | H | X | L | H | L | L | X | D _{IN} | D _{IN} |
| | H | L | H | X | L | H | H | L | X | D _{IN} | Hi-Z |
| | H | L | H | X | L | H | L | H | X | Hi-Z | D _{IN} |
| Flash Output Disable | X | H | X | H | H | X | X | X | X | Hi-Z | Hi-Z |
| | X | X | L | H | H | X | X | X | X | Hi-Z | Hi-Z |
| SRAM Output Disable | H | X | X | H | H | X | X | X | X | Hi-Z | Hi-Z |
| | H | X | X | X | X | X | H | H | X | Hi-Z | Hi-Z |
| Flash Standby | H | X | X | X | X | H | X | X | X | S | S |
| Flash Hardware Reset / Standby | X | X | X | X | X | L | X | X | X | S | S |
| SRAM Standby | X | H | X | X | X | X | X | X | X | F | F |
| | X | X | L | X | X | X | X | X | X | F | F |

Notes: L = V_{IL}; H = V_{IH}; X = V_{IH} or V_{IL}

F: Depends on flash memory operation mode.

S: Depends on SRAM operation mode.

When CIOS = V_{CC} and CIOF = V_{CC}, Word Mode is selected for both SRAM and flash memory.

Does not apply when $\overline{\text{CEF}} = \overline{\text{CE1S}} = V_{IL}$ and $\text{CE2S} = V_{IH}$ at the same time.

ID CODE TABLE

| CODE TYPE | | A20~A12 | A6 | A1 | A0 | CODE (HEX) ⁽¹⁾ |
|----------------------|-----------------|-------------------|----|----|----|---------------------------|
| Manufacturer Code | | * | L | L | L | 0098H |
| Device Code | TH50VSF2580AASB | * | L | L | H | 009AH |
| | TH50VSF2581AASB | * | L | L | H | 009CH |
| Verify Block Protect | | BA ⁽²⁾ | L | H | L | Data ⁽³⁾ |

Notes: * = V_{IH} or V_{IL}, L = V_{IL}, H = V_{IH}

(1) DQ8~DQ15 are Hi-Z in Byte mode

(2) BA: Block Address

(3) 0001H - Protected Block

0000H - Unprotected Block

COMMAND SEQUENCES

| COMMAND SEQUENCE | BUS WRITE CYCLES REQ'D | FIRST BUS WRITE CYCLE | | SECOND BUS WRITE CYCLE | | THIRD BUS WRITE CYCLE | | FOURTH BUS WRITE CYCLE | | FIFTH BUS WRITE CYCLE | | SIXTH BUS WRITE CYCLE | | |
|-----------------------|------------------------|-----------------------|-------------------------|------------------------|---------------------|-----------------------|--------------------------|------------------------|---------------------|-----------------------|------|-----------------------|-------------------|-----|
| | | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | |
| Read/Reset | 1 | XXXH | F0H | | | | | | | | | | | |
| Read/Reset | Word | 3 | 555H | AAH | 2AAH | 55H | 555H | F0H | RA ⁽¹⁾ | RD ⁽²⁾ | | | | |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| ID Read | Word | 3 | 555H | AAH | 2AAH | 55H | BK ⁽³⁾ + 555H | 90H | IA ⁽⁴⁾ | ID ⁽⁵⁾ | | | | |
| | Byte | | AAAH | | 555H | | BK ⁽³⁾ + AAH | | | | | | | |
| Auto-Program | Word | 4 | 555H | AAH | 2AAH | 55H | 555H | A0H | PA ⁽⁶⁾ | PD ⁽⁷⁾ | | | | |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Program Suspend | 1 | BK ⁽³⁾ | B0H | | | | | | | | | | | |
| Program Resume | 1 | BK ⁽³⁾ | 30H | | | | | | | | | | | |
| Auto Chip Erase | Word | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | 555H | 10H |
| | Byte | | AAAH | | 555H | | AAAH | | 555H | | AAAH | | | |
| Auto Block Erase | Word | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | BA ⁽⁸⁾ | 30H |
| | Byte | | AAAH | | 555H | | AAAH | | 555H | | AAAH | | | |
| Block Erase Suspend | 1 | BK ⁽³⁾ | B0H | | | | | | | | | | | |
| Block Erase Resume | 1 | BK ⁽³⁾ | 30H | | | | | | | | | | | |
| Block Protect | 4 | XXXH | 60H | BPA ⁽⁹⁾ | 60H | XXXH | 40H | BPA ⁽⁹⁾ | BPD ⁽¹⁰⁾ | | | | | |
| Verify Block Protect | Word | 3 | 555H | AAH | 2AAH | 55H | BK ⁽³⁾ + 555H | 90H | BPA ⁽⁹⁾ | BPD ⁽¹⁰⁾ | | | | |
| | Byte | | AAAH | | 555H | | BK ⁽³⁾ + AAH | | | | | | | |
| Fast Program Set | Word | 3 | 555H | AAH | 2AAH | 55H | 555H | 20H | | | | | | |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Fast Program | 2 | XXXH | A0H | PA ⁽⁶⁾ | PD ⁽⁷⁾ | | | | | | | | | |
| Fast Program Reset | 2 | XXXH | 90H | XXXH | F0H ⁽¹³⁾ | | | | | | | | | |
| Hidden ROM Mode Entry | Word | 3 | 555H | AAH | 2AAH | 55H | 555H | 88H | | | | | | |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Hidden ROM Program | Word | 4 | 555H | AAH | 2AAH | 55H | 555H | A0H | PA ⁽⁶⁾ | PD ⁽⁷⁾ | | | | |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Hidden ROM Erase | Word | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | BA ⁽⁸⁾ | 30H |
| | Byte | | AAAH | | 555H | | AAAH | | 555H | | AAAH | | | |
| Hidden ROM Mode Exit | Word | 4 | 555H | AAH | 2AAH | 55H | 555H | 90H | XXXH | 00H | | | | |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Query Command | Word | 2 | BK ⁽³⁾ + 55H | 98H | CA ⁽¹¹⁾ | CD ⁽¹²⁾ | | | | | | | | |
| | Byte | | BK ⁽³⁾ + AAH | | | | | | | | | | | |

Notes: The system should generate the following address patterns:

Word Mode: 555H or 2AAH on address pins A10~A0

Byte Mode: AAH or 555H on address pins A10~A0, A12F DQ8~DQ15 are ignored in Word Mode.

(1) RA: Read Address

(2) RD: Read Data

(3) BK: Bank Address = A20~A15

(4) IA: Bank Address and ID Read Address (A6, A1, A0)

Bank Address = A20~A15

Manufacturer Code = (0, 0, 0)

Device Code = (0, 0, 1)

(5) ID: ID Data

0098H - Manufacturer Code

009AH - Device Code (TH50VSF2580AASB)

009CH - Device Code (TH50VSF2581AASB)

0001H - Protected Block

• Byte mode when V_{IL} is inputted to CIOF, and addresses are A21~A0

• Write mode when V_{IH} is inputted to CIOF, and addresses are A20~A0

• Valid addresses are A10~A0 when a command is entered.

(6) PA: Program Address

(7) PD: Program Data

(8) BA: Block Address = A20~A12

(9) BPA: Block Address and ID Read Address (A6, A1, A0)

Block Address = A20~A12

ID Read Address = (0, 1, 0)

(10) BPD: Verify Data

(11) CA: CFI Address

(12) CD: CFI Data

(13) F0H: 00H is valid too

BLOCK ERASE ADDRESS TABLES

(1) TH50VSF2580AASB (top boot block)

| BANK # | BLOCK # | BLOCK ADDRESS | | | | | | | | | ADDRESS RANGE | |
|--------|---------|---------------|-----|-----|-----|-----|-----|-----|-----|-----|----------------|-----------------|
| | | BANK ADDRESS | | | | | | | | | BYTE MODE | WORD MODE |
| | | A20 | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | | |
| BK0 | BA0 | L | L | L | L | L | L | * | * | * | 00000H~00FFFFH | 00000H~007FFFH |
| | BA1 | L | L | L | L | L | H | * | * | * | 01000H~01FFFFH | 008000H~00FFFFH |
| | BA2 | L | L | L | L | H | L | * | * | * | 02000H~02FFFFH | 010000H~017FFFH |
| | BA3 | L | L | L | L | H | H | * | * | * | 03000H~03FFFFH | 018000H~01FFFFH |
| | BA4 | L | L | L | H | L | L | * | * | * | 04000H~04FFFFH | 020000H~027FFFH |
| | BA5 | L | L | L | H | L | H | * | * | * | 05000H~05FFFFH | 028000H~02FFFFH |
| | BA6 | L | L | L | H | H | L | * | * | * | 06000H~06FFFFH | 030000H~037FFFH |
| BK1 | BA7 | L | L | L | H | H | H | * | * | * | 07000H~07FFFFH | 038000H~03FFFFH |
| | BA8 | L | L | H | L | L | L | * | * | * | 08000H~08FFFFH | 040000H~047FFFH |
| | BA9 | L | L | H | L | L | H | * | * | * | 09000H~09FFFFH | 048000H~04FFFFH |
| | BA10 | L | L | H | L | H | L | * | * | * | 0A000H~0AFFFFH | 050000H~057FFFH |
| | BA11 | L | L | H | L | H | H | * | * | * | 0B000H~0BFFFFH | 058000H~05FFFFH |
| | BA12 | L | L | H | H | L | L | * | * | * | 0C000H~0CFFFFH | 060000H~067FFFH |
| | BA13 | L | L | H | H | L | H | * | * | * | 0D000H~0DFFFFH | 068000H~06FFFFH |
| BK2 | BA14 | L | L | H | H | H | L | * | * | * | 0E000H~0EFFFFH | 070000H~077FFFH |
| | BA15 | L | L | H | H | H | H | * | * | * | 0F000H~0FFFFH | 078000H~07FFFFH |
| | BA16 | L | H | L | L | L | L | * | * | * | 10000H~10FFFFH | 080000H~087FFFH |
| | BA17 | L | H | L | L | L | H | * | * | * | 11000H~11FFFFH | 088000H~08FFFFH |
| | BA18 | L | H | L | L | H | L | * | * | * | 12000H~12FFFFH | 090000H~097FFFH |
| | BA19 | L | H | L | L | H | H | * | * | * | 13000H~13FFFFH | 098000H~09FFFFH |
| | BA20 | L | H | L | H | L | L | * | * | * | 14000H~14FFFFH | 0A0000H~0A7FFFH |
| BK3 | BA21 | L | H | L | H | L | H | * | * | * | 15000H~15FFFFH | 0A8000H~0AFFFFH |
| | BA22 | L | H | L | H | H | L | * | * | * | 16000H~16FFFFH | 0B0000H~0B7FFFH |
| | BA23 | L | H | L | H | H | H | * | * | * | 17000H~17FFFFH | 0B8000H~0BFFFFH |
| | BA24 | L | H | H | L | L | L | * | * | * | 18000H~18FFFFH | 0C0000H~0C7FFFH |
| | BA25 | L | H | H | L | L | H | * | * | * | 19000H~19FFFFH | 0C8000H~0CFFFFH |
| | BA26 | L | H | H | L | H | L | * | * | * | 1A000H~1AFFFFH | 0D0000H~0D7FFFH |
| | BA27 | L | H | H | L | H | H | * | * | * | 1B000H~1BFFFFH | 0D8000H~0DFFFFH |
| BK3 | BA28 | L | H | H | H | L | L | * | * | * | 1C000H~1CFFFFH | 0E0000H~0E7FFFH |
| | BA29 | L | H | H | H | L | H | * | * | * | 1D000H~1DFFFFH | 0E8000H~0EFFFFH |
| | BA30 | L | H | H | H | H | L | * | * | * | 1E000H~1EFFFFH | 0F0000H~0F7FFFH |
| | BA31 | L | H | H | H | H | H | * | * | * | 1F000H~1FFFFH | 0F8000H~0FFFFH |

| BANK # | BLOCK # | BLOCK ADDRESS | | | | | | | | | ADDRESS RANGE | | |
|--------|---------|---------------|-----|-----|-----|-----|-----|---|-----|-----|-----------------|-----------------|-----------|
| | | BANK ADDRESS | | | | | | | A14 | A13 | A12 | BYTE MODE | WORD MODE |
| | | A20 | A19 | A18 | A17 | A16 | A15 | | | | | | |
| BK4 | BA32 | H | L | L | L | L | L | * | * | * | 200000H~20FFFFH | 100000H~107FFFH | |
| | BA33 | H | L | L | L | L | H | * | * | * | 210000H~21FFFFH | 108000H~10FFFFH | |
| | BA34 | H | L | L | L | H | L | * | * | * | 220000H~22FFFFH | 110000H~117FFFH | |
| | BA35 | H | L | L | L | H | H | * | * | * | 230000H~23FFFFH | 118000H~11FFFFH | |
| | BA36 | H | L | L | H | L | L | * | * | * | 240000H~24FFFFH | 120000H~127FFFH | |
| | BA37 | H | L | L | H | L | H | * | * | * | 250000H~25FFFFH | 128000H~12FFFFH | |
| | BA38 | H | L | L | H | H | L | * | * | * | 260000H~26FFFFH | 130000H~137FFFH | |
| | BA39 | H | L | L | H | H | H | * | * | * | 270000H~27FFFFH | 138000H~13FFFFH | |
| BK5 | BA40 | H | L | H | L | L | L | * | * | * | 280000H~28FFFFH | 140000H~147FFFH | |
| | BA41 | H | L | H | L | L | H | * | * | * | 290000H~29FFFFH | 148000H~14FFFFH | |
| | BA42 | H | L | H | L | H | L | * | * | * | 2A0000H~2AFFFFH | 150000H~157FFFH | |
| | BA43 | H | L | H | L | H | H | * | * | * | 2B0000H~2BFFFFH | 158000H~15FFFFH | |
| | BA44 | H | L | H | H | L | L | * | * | * | 2C0000H~2CFFFFH | 160000H~167FFFH | |
| | BA45 | H | L | H | H | L | H | * | * | * | 2D0000H~2DFFFFH | 168000H~16FFFFH | |
| | BA46 | H | L | H | H | H | L | * | * | * | 2E0000H~2EFFFFH | 170000H~177FFFH | |
| | BA47 | H | L | H | H | H | H | * | * | * | 2F0000H~2FFFFFH | 178000H~17FFFFH | |
| BK6 | BA48 | H | H | L | L | L | L | * | * | * | 300000H~30FFFFH | 180000H~187FFFH | |
| | BA49 | H | H | L | L | L | H | * | * | * | 310000H~31FFFFH | 188000H~18FFFFH | |
| | BA50 | H | H | L | L | H | L | * | * | * | 320000H~32FFFFH | 190000H~197FFFH | |
| | BA51 | H | H | L | L | H | H | * | * | * | 330000H~33FFFFH | 198000H~19FFFFH | |
| | BA52 | H | H | L | H | L | L | * | * | * | 340000H~34FFFFH | 1A0000H~1A7FFFH | |
| | BA53 | H | H | L | H | L | H | * | * | * | 350000H~35FFFFH | 1A8000H~1AFFFFH | |
| | BA54 | H | H | L | H | H | L | * | * | * | 360000H~36FFFFH | 1B0000H~1B7FFFH | |
| | BA55 | H | H | L | H | H | H | * | * | * | 370000H~37FFFFH | 1B8000H~1BFFFFH | |
| BK7 | BA56 | H | H | H | L | L | L | * | * | * | 380000H~38FFFFH | 1C0000H~1C7FFFH | |
| | BA57 | H | H | H | L | L | H | * | * | * | 390000H~39FFFFH | 1C8000H~1CFFFFH | |
| | BA58 | H | H | H | L | H | L | * | * | * | 3A0000H~3AFFFFH | 1D0000H~1D7FFFH | |
| | BA59 | H | H | H | L | H | H | * | * | * | 3B0000H~3BFFFFH | 1D8000H~1DFFFFH | |
| | BA60 | H | H | H | H | L | L | * | * | * | 3C0000H~3CFFFFH | 1E0000H~1E7FFFH | |
| | BA61 | H | H | H | H | L | H | * | * | * | 3D0000H~3DFFFFH | 1E8000H~1EFFFFH | |
| | BA62 | H | H | H | H | H | L | * | * | * | 3E0000H~3EFFFFH | 1F0000H~1F7FFFH | |

| BANK # | BLOCK # | BLOCK ADDRESS | | | | | | | | | ADDRESS RANGE | | |
|--------|---------|---------------|-----|-----|-----|-----|-----|---|-----|-----|------------------|------------------|-----------|
| | | BANK ADDRESS | | | | | | | A14 | A13 | A12 | BYTE MODE | WORD MODE |
| | | A20 | A19 | A18 | A17 | A16 | A15 | | | | | | |
| BK8 | BA63 | H | H | H | H | H | H | L | L | L | 3F0000H~3F1FFFFH | 1F8000H~1F8FFFFH | |
| | BA64 | H | H | H | H | H | H | L | L | H | 3F2000H~3F3FFFFH | 1F9000H~1F9FFFFH | |
| | BA65 | H | H | H | H | H | H | L | H | L | 3F4000H~3F5FFFFH | 1FA000H~1FAFFFFH | |
| | BA66 | H | H | H | H | H | H | L | H | H | 3F6000H~3F7FFFFH | 1FB000H~1FBFFFFH | |
| | BA67 | H | H | H | H | H | H | H | L | L | 3F8000H~3F9FFFFH | 1FC000H~1FCFFFFH | |
| | BA68 | H | H | H | H | H | H | H | L | H | 3FA000H~3FBFFFFH | 1FD000H~1FDFFFFH | |
| | BA69 | H | H | H | H | H | H | H | H | L | 3FC000H~3FDFFFFH | 1FE000H~1FEFFFFH | |
| | BA70 | H | H | H | H | H | H | H | H | H | 3FE000H~3FFFFFFH | 1FF000H~1FFFFFFH | |

(2) TH50VSF2581AASB (bottom boot block)

| BANK # | BLOCK # | BLOCK ADDRESS | | | | | | | | | ADDRESS RANGE | |
|--------|---------|---------------|-----|-----|-----|-----|-----|-----|-----|-----|-------------------|-------------------|
| | | BANK ADDRESS | | | | | | | | | BYTE MODE | WORD MODE |
| | | A20 | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | | |
| BK0 | BA0 | L | L | L | L | L | L | L | L | L | 000000H~001FFFFH | 000000H~000FFFFH |
| | BA1 | L | L | L | L | L | L | L | L | H | 002000H~003FFFFH | 001000H~001FFFFH |
| | BA2 | L | L | L | L | L | L | L | H | L | 004000H~005FFFFH | 002000H~002FFFFH |
| | BA3 | L | L | L | L | L | L | L | H | H | 006000H~007FFFFH | 003000H~003FFFFH |
| | BA4 | L | L | L | L | L | L | H | L | L | 008000H~009FFFFH | 004000H~004FFFFH |
| | BA5 | L | L | L | L | L | L | H | L | H | 00A000H~00BFFFFH | 005000H~005FFFFH |
| | BA6 | L | L | L | L | L | L | H | H | L | 00C000H~00DFFFFH | 006000H~006FFFFH |
| | BA7 | L | L | L | L | L | L | H | H | H | 00E000H~00FFFFFFH | 007000H~007FFFFH |
| BK1 | BA8 | L | L | L | L | L | H | * | * | * | 010000H~01FFFFFFH | 008000H~00FFFFFFH |
| | BA9 | L | L | L | L | H | L | * | * | * | 020000H~02FFFFFFH | 010000H~017FFFFH |
| | BA10 | L | L | L | L | H | H | * | * | * | 030000H~03FFFFFFH | 018000H~01FFFFFFH |
| | BA11 | L | L | L | H | L | L | * | * | * | 040000H~04FFFFFFH | 020000H~027FFFFH |
| | BA12 | L | L | L | H | L | H | * | * | * | 050000H~05FFFFFFH | 028000H~02FFFFFFH |
| | BA13 | L | L | L | H | H | L | * | * | * | 060000H~06FFFFFFH | 030000H~037FFFFH |
| | BA14 | L | L | L | H | H | H | * | * | * | 070000H~07FFFFFFH | 038000H~03FFFFFFH |
| BK2 | BA15 | L | L | H | L | L | L | * | * | * | 080000H~08FFFFFFH | 040000H~047FFFFH |
| | BA16 | L | L | H | L | L | H | * | * | * | 090000H~09FFFFFFH | 048000H~04FFFFFFH |
| | BA17 | L | L | H | L | H | L | * | * | * | 0A0000H~0AFFFFFFH | 050000H~057FFFFH |
| | BA18 | L | L | H | L | H | H | * | * | * | 0B0000H~0BFFFFFFH | 058000H~05FFFFFFH |
| | BA19 | L | L | H | H | L | L | * | * | * | 0C0000H~0CFFFFFFH | 060000H~067FFFFH |
| | BA20 | L | L | H | H | L | H | * | * | * | 0D0000H~0DFFFFFFH | 068000H~06FFFFFFH |
| | BA21 | L | L | H | H | H | L | * | * | * | 0E0000H~0EFFFFFFH | 070000H~077FFFFH |
| | BA22 | L | L | H | H | H | H | * | * | * | 0F0000H~0FFFFFFFH | 078000H~07FFFFFFH |
| BK3 | BA23 | L | H | L | L | L | L | * | * | * | 100000H~10FFFFFFH | 080000H~087FFFFH |
| | BA24 | L | H | L | L | L | H | * | * | * | 110000H~11FFFFFFH | 088000H~08FFFFFFH |
| | BA25 | L | H | L | L | H | L | * | * | * | 120000H~12FFFFFFH | 090000H~097FFFFH |
| | BA26 | L | H | L | L | H | H | * | * | * | 130000H~13FFFFFFH | 098000H~09FFFFFFH |
| | BA27 | L | H | L | H | L | L | * | * | * | 140000H~14FFFFFFH | 0A0000H~0A7FFFFH |
| | BA28 | L | H | L | H | L | H | * | * | * | 150000H~15FFFFFFH | 0A8000H~0AFFFFFFH |
| | BA29 | L | H | L | H | H | L | * | * | * | 160000H~16FFFFFFH | 0B0000H~0B7FFFFH |
| | BA30 | L | H | L | H | H | H | * | * | * | 170000H~17FFFFFFH | 0B8000H~0BFFFFFFH |

| BANK # | BLOCK # | BLOCK ADDRESS | | | | | | | | | ADDRESS RANGE | | |
|--------|---------|---------------|-----|-----|-----|-----|-----|---|-----|-----|-----------------|------------------|-----------|
| | | BANK ADDRESS | | | | | | | A14 | A13 | A12 | BYTE MODE | WORD MODE |
| | | A20 | A19 | A18 | A17 | A16 | A15 | | | | | | |
| BK4 | BA31 | L | H | H | L | L | L | * | * | * | 180000H~18FFFFH | 0C0000H~0C7FFFFH | |
| | BA32 | L | H | H | L | L | H | * | * | * | 190000H~19FFFFH | 0C8000H~0CFFFFH | |
| | BA33 | L | H | H | L | H | L | * | * | * | 1A0000H~1AFFFFH | 0D0000H~0D7FFFFH | |
| | BA34 | L | H | H | L | H | H | * | * | * | 1B0000H~1BFFFFH | 0D8000H~0DFFFFH | |
| | BA35 | L | H | H | H | L | L | * | * | * | 1C0000H~1CFFFFH | 0E0000H~0E7FFFFH | |
| | BA36 | L | H | H | H | L | H | * | * | * | 1D0000H~1DFFFFH | 0E8000H~0EFFFFH | |
| | BA37 | L | H | H | H | H | L | * | * | * | 1E0000H~1EFFFFH | 0F0000H~0F7FFFFH | |
| | BA38 | L | H | H | H | H | H | * | * | * | 1F0000H~1FFFFFH | 0F8000H~0FFFFFH | |
| BK5 | BA39 | H | L | L | L | L | L | * | * | * | 200000H~20FFFFH | 100000H~107FFFFH | |
| | BA40 | H | L | L | L | L | H | * | * | * | 210000H~21FFFFH | 108000H~10FFFFH | |
| | BA41 | H | L | L | L | H | L | * | * | * | 220000H~22FFFFH | 110000H~117FFFFH | |
| | BA42 | H | L | L | L | H | H | * | * | * | 230000H~23FFFFH | 118000H~11FFFFH | |
| | BA43 | H | L | L | H | L | L | * | * | * | 240000H~24FFFFH | 120000H~127FFFFH | |
| | BA44 | H | L | L | H | L | H | * | * | * | 250000H~25FFFFH | 128000H~12FFFFH | |
| | BA45 | H | L | L | H | H | L | * | * | * | 260000H~26FFFFH | 130000H~137FFFFH | |
| | BA46 | H | L | L | H | H | H | * | * | * | 270000H~27FFFFH | 138000H~13FFFFH | |
| BK6 | BA47 | H | L | H | L | L | L | * | * | * | 280000H~28FFFFH | 140000H~147FFFFH | |
| | BA48 | H | L | H | L | L | H | * | * | * | 290000H~29FFFFH | 148000H~14FFFFH | |
| | BA49 | H | L | H | L | H | L | * | * | * | 2A0000H~2AFFFFH | 150000H~157FFFFH | |
| | BA50 | H | L | H | L | H | H | * | * | * | 2B0000H~2BFFFFH | 158000H~15FFFFH | |
| | BA51 | H | L | H | H | L | L | * | * | * | 2C0000H~2CFFFFH | 160000H~167FFFFH | |
| | BA52 | H | L | H | H | L | H | * | * | * | 2D0000H~2DFFFFH | 168000H~16FFFFH | |
| | BA53 | H | L | H | H | H | L | * | * | * | 2E0000H~2EFFFFH | 170000H~177FFFFH | |
| | BA54 | H | L | H | H | H | H | * | * | * | 2F0000H~2FFFFFH | 178000H~17FFFFH | |
| BK7 | BA55 | H | H | L | L | L | L | * | * | * | 300000H~30FFFFH | 180000H~187FFFFH | |
| | BA56 | H | H | L | L | L | H | * | * | * | 310000H~31FFFFH | 188000H~18FFFFH | |
| | BA57 | H | H | L | L | H | L | * | * | * | 320000H~32FFFFH | 190000H~197FFFFH | |
| | BA58 | H | H | L | L | H | H | * | * | * | 330000H~33FFFFH | 198000H~19FFFFH | |
| | BA59 | H | H | L | H | L | L | * | * | * | 340000H~34FFFFH | 1A0000H~1A7FFFFH | |
| | BA60 | H | H | L | H | L | H | * | * | * | 350000H~35FFFFH | 1A8000H~1AFFFFH | |
| | BA61 | H | H | L | H | H | L | * | * | * | 360000H~36FFFFH | 1B0000H~1B7FFFFH | |
| | BA62 | H | H | L | H | H | H | * | * | * | 370000H~37FFFFH | 1B8000H~1BFFFFH | |

| BANK # | BLOCK # | BLOCK ADDRESS | | | | | | | | | ADDRESS RANGE | | |
|--------|---------|---------------|-----|-----|-----|-----|-----|---|-----|-----|-----------------|-----------------|-----------|
| | | BANK ADDRESS | | | | | | | A14 | A13 | A12 | BYTE MODE | WORD MODE |
| | | A20 | A19 | A18 | A17 | A16 | A15 | | | | | | |
| BK8 | BA63 | H | H | H | L | L | L | * | * | * | 380000H~38FFFFH | 1C0000H~1C7FFFH | |
| | BA64 | H | H | H | L | L | H | * | * | * | 390000H~39FFFFH | 1C8000H~1CFFFFH | |
| | BA65 | H | H | H | L | H | L | * | * | * | 3A0000H~3AFFFFH | 1D0000H~1D7FFFH | |
| | BA66 | H | H | H | L | H | H | * | * | * | 3B0000H~3BFFFFH | 1D8000H~1DFFFFH | |
| | BA67 | H | H | H | H | L | L | * | * | * | 3C0000H~3CFFFFH | 1E0000H~1E7FFFH | |
| | BA68 | H | H | H | H | L | H | * | * | * | 3D0000H~3DFFFFH | 1E8000H~1EFFFFH | |
| | BA69 | H | H | H | H | H | L | * | * | * | 3E0000H~3EFFFFH | 1F0000H~1F7FFFH | |
| | BA70 | H | H | H | H | H | H | * | * | * | 3F0000H~3FFFFFH | 1F8000H~1FFFFFH | |

BLOCK SIZE TABLE

(1) TH50VSF2580AASB (top boot block)

| BLOCK # | BLOCK SIZE | | BANK # | BANK SIZE | | BLOCK COUNT |
|-----------|------------|-----------|--------|------------|------------|-------------|
| | BYTE MODE | WORD MODE | | BYTE MODE | WORD MODE | |
| BA0~BA7 | 64 Kbytes | 32 Kwords | BK0 | 512 Kbytes | 256 Kwords | 8 |
| BA8~BA15 | 64 Kbytes | 32 Kwords | BK1 | 512 Kbytes | 256 Kwords | 8 |
| BA16~BA23 | 64 Kbytes | 32 Kwords | BK2 | 512 Kbytes | 256 Kwords | 8 |
| BA24~BA31 | 64 Kbytes | 32 Kwords | BK3 | 512 Kbytes | 256 Kwords | 8 |
| BA32~BA39 | 64 Kbytes | 32 Kwords | BK4 | 512 Kbytes | 256 Kwords | 8 |
| BA40~BA47 | 64 Kbytes | 32 Kwords | BK5 | 512 Kbytes | 256 Kwords | 8 |
| BA48~BA55 | 64 Kbytes | 32 Kwords | BK6 | 512 Kbytes | 256 Kwords | 8 |
| BA56~BA62 | 64 Kbytes | 32 Kwords | BK7 | 448 Kbytes | 224 Kwords | 7 |
| BA63~BA70 | 8 Kbytes | 4 Kwords | BK8 | 64 Kbytes | 32 Kwords | 8 |

(2) TH50VSF2581AASB (bottom boot block)

| BLOCK # | BLOCK SIZE | | BANK # | BANK SIZE | | BLOCK COUNT |
|-----------|------------|-----------|--------|------------|------------|-------------|
| | BYTE MODE | WORD MODE | | BYTE MODE | WORD MODE | |
| BA0~BA7 | 8 Kbytes | 4 Kwords | BK0 | 64 Kbytes | 32 Kwords | 8 |
| BA8~BA14 | 64 Kbytes | 32 Kwords | BK1 | 448 Kbytes | 224 Kwords | 7 |
| BA15~BA22 | 64 Kbytes | 32 Kwords | BK2 | 512 Kbytes | 256 Kwords | 8 |
| BA23~BA30 | 64 Kbytes | 32 Kwords | BK3 | 512 Kbytes | 256 Kwords | 8 |
| BA31~BA38 | 64 Kbytes | 32 Kwords | BK4 | 512 Kbytes | 256 Kwords | 8 |
| BA39~BA46 | 64 Kbytes | 32 Kwords | BK5 | 512 Kbytes | 256 Kwords | 8 |
| BA47~BA54 | 64 Kbytes | 32 Kwords | BK6 | 512 Kbytes | 256 Kwords | 8 |
| BA55~BA62 | 64 Kbytes | 32 Kwords | BK7 | 512 Kbytes | 256 Kwords | 8 |
| BA63~BA70 | 64 Kbytes | 32 Kwords | BK8 | 512 Kbytes | 256 Kwords | 8 |

ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RANGE | UNIT |
|---------------------|---|------------------------------------|--------|
| V _{CC} | V _{CCs} /V _{CCf} Supply Voltage | -0.3~4.6 | V |
| V _{IN} | Input Voltage ⁽¹⁾ | -0.3~4.6 | V |
| V _{DQ} | Input/Output Voltage | -0.5~V _{CC} + 0.5 (≤ 4.6) | V |
| T _{opr} | Operating Temperature | -40~85 | °C |
| P _D | Power Dissipation | 0.6 | W |
| T _{solder} | Soldering Temperature (10s) | 260 | °C |
| I _{OSHORT} | Output Short Circuit Current ⁽²⁾ | 100 | mA |
| N _{EW} | Erase/Program Cycling Capability | 100,000 | Cycles |
| T _{stg} | Storage Temperature | -55~125 | °C |

(1) -2.0 V for pulse width ≤ 20 ns

(2) Output shorted for no more than one second. No more than one output shorted at a time

HARDWARE SEQUENCE FLAGS

| STATUS | | | DQ7 | DQ6 | DQ5 | DQ3 | DQ2 | RY/ $\overline{\text{BY}}$ | |
|---------------------|--|-----------------|-----------------------------|--------|--------|------|--------|----------------------------|------|
| In Progress | Auto Programming | | $\overline{\text{DQ7}}$ | Toggle | 0 | 0 | 1 | 0 | |
| | Read in Program Suspend ⁽¹⁾ | | Data | Data | Data | Data | Data | Hi-Z | |
| | In Auto Erase | Erase Hold Time | Selected ⁽²⁾ | 0 | Toggle | 0 | 0 | Toggle | 0 |
| | | | Not-selected ⁽³⁾ | 0 | Toggle | 0 | 0 | 1 | 0 |
| | | Auto Erase | Selected | 0 | Toggle | 0 | 1 | Toggle | 0 |
| | | | Not-selected | 0 | Toggle | 0 | 1 | 1 | 0 |
| | In Erase Suspend | Read | Selected | 1 | 1 | 0 | 0 | Toggle | Hi-Z |
| | | | Not-selected | Data | Data | Data | Data | Data | Hi-Z |
| Programming | | Selected | $\overline{\text{DQ7}}$ | Toggle | 0 | 0 | Toggle | 0 | |
| | | Not-selected | $\overline{\text{DQ7}}$ | Toggle | 0 | 0 | 1 | 0 | |
| Time Limit Exceeded | Auto Programming | | $\overline{\text{DQ7}}$ | Toggle | 1 | 0 | 1 | 0 | |
| | Auto Erase | | 0 | Toggle | 1 | 1 | NA | 0 | |
| | Programming in Erase Suspend | | $\overline{\text{DQ7}}$ | Toggle | 1 | 0 | NA | 0 | |

Notes: DQ outputs cell data and $\overline{\text{RY/BY}}$ goes High-Impedence when the operation has been completed.

DQ0 and DQ1 pins are reserved for future use.

0 is output on DQ0, DQ1 and DQ4.

(1) Data output from an address to which Write is being performed are undefined.

(2) Output when the block address selected for Auto Block Erase is specified and data is read from there.

During Auto Chip Erase, all blocks are selected.

(3) Output when a block address not selected for Auto Block Erase of same bank as selected block is specified and data is read from there.

RECOMMENDED DC OPERATING CONDITIONS (Ta = -40°~85°C)

| SYMBOL | PARAMETER | MIN | TYP. | MAX | UNIT |
|------------------------------------|--------------------------------------|---------------------|------|-----------------------|------|
| V _{CCs} /V _{CCf} | Power Supply Voltage | 2.7 | — | 3.6 | V |
| V _{IH} | Input High-Level Voltage | 2.2 | — | V _{CC} + 0.3 | |
| V _{IL} | Input Low-Level Voltage | -0.3 ⁽¹⁾ | — | V _{CC} × 0.2 | |
| V _{DH} | Data Retention Voltage for SRAM | 1.5 | — | 3.6 | |
| V _{LKO} | Flash Low-Lock Voltage | 2.3 | — | 2.5 | |
| V _{ACC} | High Voltage for $\overline{WP/ACC}$ | 8.5 | — | 9.5 | |
| V _{ID} | High Voltage for \overline{RESET} | 11.4 | — | 12.6 | |

(1) -2.0 V for pulse width ≤ 20 ns

CAPACITANCE (Ta = 25°C, f = 1 MHz)

| SYMBOL | PARAMETER | CONDITION | MIN | TYP. | MAX | UNIT |
|------------------|--------------------|---------------------------|-----|------|-----|------|
| C _{IN} | Input Capacitance | V _{IN} = GND | — | — | 15 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} GND = | — | — | 20 | pF |

Note: These parameters are sampled periodically and are not tested for every device.

DC CHARACTERISTICS (Ta = -40°~85°C, VCCs/VCCf = 2.7 V~3.6 V)

| SYMBOL | PARAMETER | CONDITIONS | | | MIN | TYP. | MAX | UNIT |
|----------------------------------|--|--|------------------------------|--------------------------------------|------|------|-----|------|
| I _{IL} | Input Leakage Current | V _{IN} = 0 V~V _{CC} | | | — | — | ±1 | μA |
| I _{SOH} | SRAM Output High Current | V _{OH} = V _{CCs} - 0.5 V | | | -0.5 | — | — | mA |
| I _{SOL} | SRAM Output Low Current | V _{OL} = 0.4 V | | | 2.1 | — | — | mA |
| I _{FOH1} | Flash Output High Current (TTL) | V _{OH} = 2.4 V | | | -0.4 | — | — | mA |
| I _{FOH2} | Flash Output High Current (CMOS) | V _{OH} = V _{CCf} × 0.85 | | | -2.5 | — | — | mA |
| | | V _{OH} = V _{CCf} - 0.4 V | | | -100 | — | — | μA |
| I _{FOL} | Flash Output Low Current | V _{OL} = 0.4 V | | | 4 | — | — | mA |
| I _{LO} | Output Leakage Current | V _{OUT} = 0 V~V _{CC} , $\overline{OE} = V_{IH}$ | | | — | — | ±1 | μA |
| I _{CCO1} | Flash Average Read Current | $\overline{CE\overline{F}} = V_{IL}$, $\overline{OE} = V_{IH}$, I _{OUT} = 0 mA, t _{cycle} = t _{RC} (min) | | | — | — | 30 | mA |
| I _{CCO2} | Flash Average Program/Erase Current | $\overline{CE\overline{F}} = V_{IL}$, $\overline{OE} = V_{IH}$, I _{OUT} = 0 mA | | | — | — | 15 | mA |
| I _{CCO3} | SRAM Average Operating Current | $\overline{CE1\overline{S}} = V_{IL}$, CE2S = V _{IH} , $\overline{OE} = V_{IH}$, I _{OUT} = 0 mA | | t _{cycle} = t _{RC} | — | — | 50 | mA |
| | | | | t _{cycle} = 1 MHz | — | — | 12 | |
| I _{CCO4} | | $\overline{CE1\overline{S}} = 0.2\text{ V}$, $\overline{OE} = V_{CCs} - 0.2\text{ V}$, CE2S = V _{CCs} - 0.2 V, I _{OUT} = 0 mA | | t _{cycle} = t _{RC} | — | — | 45 | mA |
| | | | | t _{cycle} = 1 MHz | — | — | 5 | |
| I _{CCO5} | Flash Average Read-while-Programming Current | V _{IN} = V _{IH} /V _{IL} , I _{OUT} = 0 mA, t _{cycle} = t _{RC} (min) | | | — | — | 45 | mA |
| I _{CCO6} | Flash Average Read-while-Erasing Current | V _{IN} = V _{IH} /V _{IL} , I _{OUT} = 0 mA, t _{cycle} = t _{RC} (min) | | | — | — | 45 | mA |
| I _{CCO7} | Flash Average Program-while-Erase-Suspended Current | V _{IN} = V _{IH} /V _{IL} , I _{OUT} = 0 mA | | | — | — | 15 | mA |
| I _{CCS1} | Flash Standby Current | $\overline{CE\overline{F}} = \overline{RESET} = V_{CCf}$ or $\overline{RESET} = V_{SS}$ | | | — | — | 10 | μA |
| I _{CCS2} | Flash Standby Current (Automatic Sleep Mode ⁽¹⁾) | V _{IH} = V _{CCf} or V _{IL} = V _{SS} | | | — | — | 10 | μA |
| I _{CCS3} | SRAM Standby Current | $\overline{CE1\overline{S}} = V_{IH}$ or CE2S = V _{IL} | | | — | — | 2 | mA |
| I _{CCS4} | | $\overline{CE1\overline{S}} = V_{CCs} - 0.2\text{ V}$ or CE2S = 0.2 V ⁽²⁾ | V _{CCs} = 3.0 V | Ta = 25°C | — | 0.01 | 0.5 | |
| | | | | Ta = -20°~40°C | — | — | 1 | |
| | | | | Ta = -20°~85°C | — | — | 5 | |
| | | | V _{CCs} = 3 V ± 10% | Ta = 25°C | — | — | 0.6 | |
| | | | | Ta = -20°~85°C | — | — | 6 | |
| | Ta = 25°C | | | — | — | 0.7 | | |
| V _{CCs} = 3.3 V ± 0.3 V | Ta = 25°C | — | — | 0.7 | | | | |
| | Ta = -20°~85°C | — | — | 7 | | | | |
| I _{ACC} | High-Voltage Input Current for WP/ACC | 8.5 V ≤ V _{ACC} ≤ 9.5 V | | | — | — | 20 | mA |

(1) If the address remains unchanged for 150 ns, the device will enter Automatic Sleep Mode.

(2) In Standby Mode, with $\overline{CE1\overline{S}} \geq V_{CCs} - 0.2\text{ V}$, these limits are guaranteed when CE2S ≥ V_{CCs} - 0.2 V or CE2S ≤ 0.2 V, and CIOs ≥ V_{CCs} - 0.2 V or CIOs ≤ 0.2 V.

AC CHARACTERISTICS (SRAM) (Ta = -40°~85°C, VCCs = 2.7 V~3.6 V)

Read cycle

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|------------------|--|-----|-----|------|
| t _{RC} | Read Cycle Time | 90 | — | ns |
| t _{ACC} | Address Access Time | — | 90 | |
| t _{CO1} | Chip Enable (CE1S) Access Time | — | 90 | |
| t _{CO2} | Chip Enable (CE2S) Access Time | — | 90 | |
| t _{OE} | Output Enable Access Time | — | 45 | |
| t _{BA} | Data Byte Control Access Time | — | 45 | |
| t _{COE} | Chip Enable Low to Output Active | 5 | — | |
| t _{OEE} | Output Enable Low to Output Active | 0 | — | |
| t _{BE} | Data Byte Control Low to Output Active | 0 | — | |
| t _{OD} | Chip Enable High to Output Hi-Z | — | 35 | |
| t _{ODO} | Output Enable High to Output Hi-Z | — | 35 | |
| t _{BD} | Data Byte Control High to Output Hi-Z | — | 35 | |
| t _{OH} | Output Data Hold Time | 10 | — | |
| t _{CCR} | CE Recovery Time | 0 | — | |

Write cycle

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|------------------|---------------------------------------|-----|-----|------|
| t _{WC} | Write Cycle Time | 85 | — | ns |
| t _{WP} | Write Pulse Width | 55 | — | |
| t _{CW} | Chip Enable to End of Write | 70 | — | |
| t _{BW} | Data Byte Control to End of Write | 55 | — | |
| t _{AS} | Address Set-up Time | 0 | — | |
| t _{WR} | Write Recovery Time | 0 | — | |
| t _{ODW} | \overline{WE} Low to Output Hi-Z | — | 35 | |
| t _{OEW} | \overline{WE} High to Output Active | 0 | — | |
| t _{DS} | Data Set-up Time | 35 | — | |
| t _{DH} | Data Hold Time | 0 | — | |

AC TEST CONDITIONS

| PARAMETER | VALUES |
|---|------------------------------------|
| Input Pulse Level | 0.4 V, 2.4 V |
| Input Pulse Rise and Fall Time (10%~90%) | 5 ns |
| Timing Measurement Reference Level (input) | V _{CCs} × 0.5 |
| Timing Measurement Reference Level (output) | V _{CCs} × 0.5 |
| Output Load | C _L (30pF) + 1 TTL gate |

AC CHARACTERISTICS (FLASH MEMORY)

READ CYCLE

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|-----------|---|-----|-----|------|
| t_{RC} | Read Cycle Time | 90 | — | ns |
| t_{ACC} | Address Access Time | — | 90 | ns |
| t_{CE} | $\overline{CE\overline{F}}$ Access Time | — | 90 | ns |
| t_{OE} | \overline{OE} Access Time | — | 40 | ns |
| t_{CEE} | $\overline{CE\overline{F}}$ to Output Low-Z | 0 | — | ns |
| t_{OEE} | \overline{OE} to Output Low-Z | 0 | — | ns |
| t_{OEH} | \overline{OE} Hold Time | 0 | — | ns |
| t_{OH} | Output Data Hold Time | 0 | — | ns |
| t_{DF1} | $\overline{CE\overline{F}}$ to Output Hi-Z | — | 30 | ns |
| t_{DF2} | \overline{OE} to Output Hi-Z | — | 30 | ns |

BLOCK PROTECT

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|------------|---|-----|-----|---------|
| t_{VPS} | V_{ID} Set-up Time | 4 | — | μs |
| t_{CESP} | $\overline{CE\overline{F}}$ Set-up Time | 4 | — | μs |
| t_{VPH} | \overline{OE} Hold Time | 4 | — | μs |
| t_{PPLH} | \overline{WE} Low-Level Hold Time | 100 | — | μs |

PROGRAM AND ERASE CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|------------|-------------------------------|--------|-----|---------|
| t_{PPW} | Auto-Program Time (Byte Mode) | 8* | 300 | μs |
| | Auto-Program Time (Word Mode) | 11* | 300 | μs |
| t_{PCEW} | Auto Chip Erase Time | 50* | 710 | s |
| t_{PBEW} | Auto Block Erase Time | 0.7* | 10 | s |
| t_{EW} | Erase/Program Cycle | 10^5 | — | Cycles |

*: typ.

COMMAND WRITE/PROGRAM/ERASE CYCLE

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------------------|---|-----|-----|------|
| t _{CMD} | Command Write Cycle Time | 120 | — | ns |
| t _{AS} | Address Set-up Time / $\overline{\text{BYTE}}$ Set-up Time | 0 | — | ns |
| t _{AH} | Address Hold Time / $\overline{\text{BYTE}}$ Hold Time | 50 | — | ns |
| t _{AHW} | Address Hold Time from $\overline{\text{WE}}$ High level | 20 | — | ns |
| t _{DS} | Data Set-up Time | 50 | — | ns |
| t _{DH} | Data Hold Time | 0 | — | ns |
| t _{WELH} | $\overline{\text{WE}}$ Low-Level Hold Time ($\overline{\text{WE}}$ Control) | 50 | — | ns |
| t _{WEHH} | $\overline{\text{WE}}$ High-Level Hold Time ($\overline{\text{WE}}$ Control) | 20 | — | ns |
| t _{CES} | $\overline{\text{CE}}$ Set-up Time to $\overline{\text{WE}}$ Active ($\overline{\text{WE}}$ Control) | 0 | — | ns |
| t _{CEH} | $\overline{\text{CE}}$ Hold Time from $\overline{\text{WE}}$ High Level ($\overline{\text{WE}}$ Control) | 0 | — | ns |
| t _{CELH} | $\overline{\text{CE}}$ Low-Level Hold Time ($\overline{\text{CE}}$ Control) | 50 | — | ns |
| t _{CEHH} | $\overline{\text{CE}}$ High-Level Hold Time ($\overline{\text{CE}}$ Control) | 20 | — | ns |
| t _{WES} | $\overline{\text{WE}}$ Set-up time to $\overline{\text{CE}}$ Active ($\overline{\text{CE}}$ Control) | 0 | — | ns |
| t _{WEH} | $\overline{\text{WE}}$ Hold Time from $\overline{\text{CE}}$ High Level ($\overline{\text{CE}}$ Control) | 0 | — | ns |
| t _{OES} | $\overline{\text{OE}}$ Set-up Time | 0 | — | ns |
| t _{OEHP} | $\overline{\text{OE}}$ Hold Time (Toggle, Data Polling) | 90 | — | ns |
| t _{OEHT} | $\overline{\text{OE}}$ High-Level Hold Time (Toggle) | 20 | — | ns |
| t _{AST} | Address Set-up Time (Toggle) | 0 | | ns |
| t _{AHT} | Address Hold Time (toggle) | 0 | | ns |
| t _{BEH} | Erase Hold Time | 50 | — | μs |
| t _{VCS} | V _{CCf} Set-up Time | 500 | — | μs |
| t _{BUSY} | Program/Erase Valid to $\overline{\text{RY}}/\overline{\text{BY}}$ Delay | — | 90 | ns |
| t _{RP} | $\overline{\text{RESET}}$ Low-Level Hold Time | 500 | — | ns |
| t _{READY} | $\overline{\text{RESET}}$ Low-Level to Read Mode | — | 20 | μs |
| t _{RB} | $\overline{\text{RY}}/\overline{\text{BY}}$ Recovery Time | 0 | — | ns |
| t _{RH} | $\overline{\text{RESET}}$ Recovery Time | 50 | — | ns |
| t _{CEBTS} | $\overline{\text{CE}}$ Set-up time $\overline{\text{BYTE}}$ Transition | 5 | — | ns |
| t _{SUSP} | Program Suspend Command to Suspend Mode | — | 1.5 | μs |
| t _{RESP} | Program Resume Command to Program Mode | — | 1 | μs |
| t _{SUSE} | Erase Suspend Command to Suspend Mode | — | 15 | μs |
| t _{RESE} | Erase Resume Command to Erase Mode | — | 1 | μs |

SIMULTANEOUS READ/WRITE OPERATION

The TH50VSF2580/2581AASB features a Simultaneous Read/Write operation. The Simultaneous Read/Write operation enables the device to simultaneously write data to or erase data from a bank while reading data from another bank.

The TH50VSF2580/2581AASB has a total of nine banks: 1 bank of 0.5 Mbits, 1 bank of 3.5 Mbits and 7 banks of 4 Mbits. Banks can be switched between using the bank addresses (A20~A15). For a description of bank blocks and addresses, please refer to the Block Address Table and Block Size Table.

The Simultaneous Read/Write operation cannot perform multiple operations within a single bank. The table below shows the operation modes in which simultaneous operation can be performed.

Note that during Auto-Program execution or Auto Block Erase operation, the Simultaneous Read/Write operation cannot read data from addresses in the same bank which have not been selected for operation. Data from these addresses can be read using the Program Suspend or Erase Suspend function, however.

SIMULTANEOUS READ/WRITE OPERATION

| STATUS OF BANK ON WHICH OPERATION IS BEING PERFORMED | STATUS OF OTHER BANKS |
|--|-----------------------|
| Read Mode | Read Mode |
| ID Read Mode ⁽¹⁾ | |
| Auto-Program Mode | |
| Fast Program Mode ⁽²⁾ | |
| Program Suspend Mode | |
| Auto Block Erase Mode | |
| Auto Multiple Block Erase Mode ⁽³⁾ | |
| Erase Suspend Mode | |
| Program Suspend during Erase Suspend | |
| CFI Mode | |

(1) Only Command Mode is valid.

(2) Including times when Acceleration Mode is in use.

(3) If the selected blocks are spread across all nine banks, simultaneous operation cannot be carried out.

OPERATION MODES

In addition to the Read, Write and Erase Modes, the TH50VSF2520/2581AASB features many functions including block protection and data polling. When incorporating the device into a design, please refer to the timing charts and flowcharts in combination with the description below.

Read Mode

To read data from the memory cell array, set the device to Read Mode. In Read Mode the device can perform high-speed random access as asynchronous ROM.

The device is automatically set to Read Mode immediately after power-on or on completion of automatic operation. A software reset releases ID Read Mode and the lock state which the device enters if automatic operation ends abnormally, and sets the device to Read Mode. A hardware reset terminates operation of the device and resets it to Read Mode. When reading data without changing the address immediately after power-on, either input a hardware Reset or change $\overline{\text{CEF}}$ from H to L.

ID Read Mode

ID Read mode is used to read the device maker code and device code. The mode is useful for EPROM programmers to automatically identify the device type.

In this method, simultaneous operation can be performed. Inputting an ID Read command sets the specified bank to ID Read mode. Banks are specified by inputting the bank address (BK) in the third bus write cycle of the command cycle. To read an ID code, the bank address as well as the ID read address must be specified. From address BK + 00 the maker code is output; from address BK + 01 the device code is output. From other banks, data are output from the memory cells. Inputting a Reset command releases ID Read mode and returns the device to Read mode.

Access time in ID Read mode is the same as that in Read mode. For the codes, see the ID Code Table.

Standby Mode

There are two ways to put the device into Standby Mode.

- (1) Control using $\overline{CE\overline{F}}$ and $\overline{RESE\overline{T}}$

With the device in Read Mode, input $V_{DD} \pm 0.3$ V to $\overline{CE\overline{F}}$ and $\overline{RESE\overline{T}}$. The device will enter Standby Mode and the current will be reduced to the standby current (I_{CCS1}). However, if the device is in the process of performing simultaneous operation, the device will not enter Standby Mode but will instead cause the operating current to flow.

- (2) Control using $\overline{RESE\overline{T}}$ only

With the device in Read Mode, input $V_{SS} \pm 0.3$ V to $\overline{RESE\overline{T}}$. The device will enter Standby Mode and the current will be reduced to the standby current (I_{CCS1}). Even if the device is in the process of performing simultaneous operation, this method will terminate the current operation and set the device to Standby Mode. This is a hardware reset and is described later.

In Standby Mode DQ is put in High-Impedance state.

Auto-Sleep Mode

This function suppresses power dissipation during reading. If the address input does not change for 150 ns, the device will automatically enter Sleep Mode and the current will be reduced to the standby current (I_{CCS2}). However, if the device is in the process of performing simultaneous operation, the device will not enter Standby Mode but will instead cause the operating current to flow. Because the output data is latched, data is output in Sleep Mode. When the address is changed, Sleep Mode is automatically released, and data from the new address is output.

Output Disable Mode

Inputting V_{IH} to \overline{OE} disables output from the device and sets DQ to High-Impedance.

Command Write

The TH50VSF2580/2581AASB uses the standard JEDEC control commands for a single-power supply E²PROM. A Command Write is executed by inputting the address and data into the Command Register. The command is written by inputting a pulse to \overline{WE} with $\overline{CE\overline{F}} = V_{IL}$ and $\overline{OE} = V_{IH}$ (\overline{WE} control). The command can also be written by inputting a pulse to $\overline{CE\overline{F}}$ with $\overline{WE} = V_{IL}$ ($\overline{CE\overline{F}}$ control). The address is latched on the falling edge of either \overline{WE} or $\overline{CE\overline{F}}$. The data is latched on the rising edge of either \overline{WE} or $\overline{CE\overline{F}}$. DQ0~DQ7 are valid for data input and DQ8~DQ15 are ignored.

To abort input of the command sequence use the Reset command. The device will reset the Command Register and enter Read Mode. If an undefined command is input, the Command Register will be reset and the device will enter Read Mode.

Software Reset

Apply a software reset by inputting a Read/Reset command. A software reset returns the device from ID Read Mode or CFI Mode to Read Mode, releases the lock state if automatic operation has ended abnormally, and clears the Command Register.

Hardware Reset

A hardware reset initializes the device and sets it to Read Mode. When a pulse is input to \overline{RESET} for t_{RP} , the device abandons the operation which is in progress and enters Read Mode after t_{READY} . Note that if a hardware reset is applied during data overwriting, such as a Write or Erase operation, data at the address or block being written to at the time of the reset will become undefined.

After a hardware reset the device enters Read Mode if $\overline{RESET} = V_{IH}$ or Standby Mode if $\overline{RESET} = V_{IL}$. The DQ pins are High-Impedance when $\overline{RESET} = V_{IL}$. After the device has entered Read Mode, Read operations and input of any command are allowed.

Comparison between Software Reset and Hardware Reset

| ACTION | SOFTWARE RESET | HARDWARE RESET |
|---|----------------|----------------|
| Releases ID Read Mode or CFI Mode. | True | True |
| Clears the Command Register. | True | True |
| Releases the lock state if automatic operation has ended abnormally. | True | True |
| Stops any automatic operation which is in progress. | False | True |
| Stops any operation other than the above and returns the device to Read Mode. | False | True |

\overline{BYTE} /Word Mode

CIOF is used select Word Mode (16 bits) or Byte Mode (8 bits) for the TH50VSF2580/2581AASB. If V_{IH} is input to CIOF, the device will operate in Word Mode. Read data or write commands using DQ0~DQ15. When V_{IL} is input to CIOF, read data or write commands using DQ0~DQ7. A12F is used as the lowest address. DQ8~DQ14 will become High-Impedance.

Auto-Program Mode

The TH50VSF2580/2581AASB can be programmed in either byte or word units. Auto-Program Mode is set using the Program command. The program address is latched on the falling edge of the \overline{WE} signal and data is latched on the rising edge of the fourth Bus Write cycle (with \overline{WE} control). Auto programming starts on the rising edge of the \overline{WE} signal in the fourth Bus Write cycle. The Program and Program Verify commands are automatically executed by the chip. The device status during programming is indicated by the Hardware Sequence flag. To read the Hardware Sequence flag, specify the address to which the Write is being performed.

During Auto-Program execution, a command sequence for the bank on which execution is being performed cannot be accepted. To terminate execution, use a hardware reset. Note that if the Auto-Program operation is terminated in this manner, the data written so far is invalid.

Any attempt to program a protected block is ignored. In this case the device enters Read Mode 3 μ s after the rising edge of the \overline{WE} signal in the fourth Bus Write cycle.

If an Auto-Program operation fails, the device remains in the programming state and does not automatically return to Read Mode. The device status is indicated by the Hardware Sequence flag. Either a Reset command or a hardware reset is required to return the device to Read Mode after a failure. If a programming operation fails, the block which contains the address to which data could not be programmed should not be used.

The device allows 0s to be programmed into memory cells which contain a 1. 1s cannot be programmed into cells which contain 0s. If this is attempted, execution of Auto Program will fail. This is a user error, not a device error. A cell containing 0 must be erased in order to set it to 1.

Fast Program Mode

Fast Program is a function which enables execution of the command sequence for the Auto Program to be completed in two cycles. In this mode the first two cycles of the command sequence, which normally requires four cycles, are omitted. Writing is performed in the remaining two cycles. To execute Fast Program, input the Fast Program command. Write in this mode uses the Fast Program command but operation is the same as that for ordinary Auto-Program. The status of the device is indicated by the Hardware Sequence flag and read operations can be performed as usual. To exit this mode, the Fast Program Reset command must be input. When the command is input, the device will return to Read Mode.

Acceleration Mode

The TH50VSF2580/2581AASB features Acceleration Mode which allows write time to be reduced. Applying V_{ACC} to \overline{WP} or ACC automatically sets the device to Acceleration Mode. In Acceleration Mode, Block Protect Mode changes to Temporary Block Unprotect Mode. Write Mode changes to Fast Program Mode. Modes are switched by the \overline{WP}/ACC signal; thus, there is no need for a Temporary Block Unprotect operation or to set or reset Fast Program Mode. Operation of Write is the same as in Auto-Program Mode. Removing V_{ACC} from \overline{WP}/ACC terminates Acceleration Mode.

Program Suspend/Resume Mode

Program Suspend is used to enable Data Read by suspending the Write operation. The device accepts a Program Suspend command in Write Mode (including Write operations performed during Erase Suspend) but ignores the command in other modes. When the command is input, the address of the bank on which Write is being performed must be specified. After input of the command, the device will enter Program Suspend Read Mode after t_{SUSP} .

During Program Suspend, Cell Data Read, ID Read and CFI Data Read can be performed. When Data Write is suspended, the address to which Write was being performed becomes undefined. ID Read and CFI Data Read are the same as usual.

After completion of Program Suspend input a Program Resume command to return to Write Mode. When inputting the command, specify the address of the bank on which Write is being performed. If the ID Read or CFI Data Read functions is being used, abort the function before inputting the Resume command. On receiving the Resume command, the device returns to Write Mode and resumes outputting the Hardware Sequence flag for the bank to which data is being written.

Program Suspend can be run in Fast Program Mode or Acceleration Mode. However, note that when running Program Suspend in Acceleration Mode, V_{ACC} must not be released.

Auto Chip Erase Mode

The Auto Chip Erase Mode is set using the Chip Erase command. An Auto Chip Erase operation starts on the rising edge of \overline{WE} in the sixth bus cycle. All memory cells are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is indicated by the Hardware Sequence flag.

Command input is ignored during an Auto Chip Erase. A hardware reset can interrupt an Auto Chip Erase operation. If an Auto Chip Erase operation is interrupted, it cannot be completed correctly. Hence an additional Erase operation must be performed.

Any attempt to erase a protected block is ignored. If all blocks are protected, the Auto Erase operation will not be executed and the device will enter Read mode 100 μ s after the rising edge of the \overline{WE} signal in the sixth bus cycle.

If an Auto Chip Erase operation fails, the device will remain in the erasing state and will not return to Read Mode. The device status is indicated by the Hardware Sequence flag. Either a Reset command or a hardware reset is required to return the device to Read Mode after a failure.

In this case it cannot be ascertained which block the failure occurred in. Either abandon use of the device altogether, or perform a Block Erase on each block, identify the failed block, and stop using it. The host processor must take measures to prevent subsequent use of the failed block.

Auto Block Erase / Auto Multi-Block Erase Modes

The Auto Block Erase Mode and Auto Multi-Block Erase Mode are set using the Block Erase command. The block address is latched on the falling edge of the \overline{WE} signal in the sixth bus cycle. The block erase starts as soon as the Erase Hold Time (t_{BEH}) has elapsed after the rising edge of the \overline{WE} signal. When multiple blocks are erased, the sixth Bus Write cycle is repeated with each block address and Auto Block Erase command being input within the Erase Hold Time (this constitutes an Auto Multi-Block Erase operation). If a command other than an Auto Block Erase command or Erase Suspend command is input during the Erase Hold Time, the device will reset the Command Register and enter Read Mode. The Erase Hold Time restarts on each successive rising edge of \overline{WE} . Once operation starts, all memory cells in the selected block are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is indicated by the setting of the Hardware Sequence flag. When the Hardware Sequence flag is read, the addresses of the blocks on which auto-erase operation is being performed must be specified. If the selected blocks are spread across all nine banks, simultaneous operation cannot be carried out.

All commands (except Erase Suspend) are ignored during an Auto Block Erase or Auto Multi-Block Erase operation. Either operation can be aborted using a Hardware Reset. If an auto-erase operation is interrupted, it cannot be completed correctly; therefore, a further erase operation is necessary to complete the erasing.

Any attempt to erase a protected block is ignored. If all the selected blocks are protected, the auto-erase operation is not executed and the device returns to Read Mode 100 μ s after the rising edge of the \overline{WE} signal in the last bus cycle.

If an auto-erase operation fails, the device remains in Erasing state and does not return to Read Mode. The device status is indicated by the Hardware Sequence flag. After a failure either a Reset command or a Hardware Reset is required to return the device to Read Mode. If multiple blocks are selected, it will not be possible to ascertain the block in which the failure occurred. In this case either abandon use of the device altogether, or perform a Block Erase on each block, identify the failed block, and stop using it. The host processor must take measures to prevent subsequent use of the failed block.

Erase Suspend / Erase Resume Modes

Erase Suspend Mode suspends Auto Block Erase and reads data from or writes data to an unselected block. The Erase Suspend command is allowed during an auto block erase operation but is ignored in all other operation modes. When the command is input, the address of the bank on which Erase is being performed must be specified.

In Erase Suspend Mode only a Read, Program or Resume command can be accepted. If an Erase Suspend command is input during an Auto Block Erase, the device will enter Erase Suspend Read Mode after t_{SUSE} . The device status (Erase Suspend Read Mode) can be verified by checking the Hardware Sequence flag. If data is read consecutively from the block selected for Auto Block Erase, the DQ2 output will toggle and the DQ6 output will stop toggling and $\overline{RY/BY}$ will be set to High-Impedance.

Inputting a Write command during an Erase Suspend enables a Write to be performed to a block which has not been selected for the Auto Block Erase. Data is written in the usual manner.

To resume the Auto Block Erase, input an Erase Resume command. On input of the command, the address of the bank on which the Write was being performed must be specified. On receiving an Erase Resume command, the device returns to the state it was in when the Erase Suspend command was input. If an Erase Suspend command is input during the Erase Hold Time, the device will return to the state it was in at the start of the Erase Hold Time. At this time more blocks can be specified for erasing. If an Erase Resume command is input during an Auto Block Erase, Erase resumes. At this time toggle output of DQ6 resumes and 0 is output on $\overline{RY/BY}$.

Block Protection

Block Protection is a function to disable write and erase in block units. Applying VID to $\overline{\text{RESET}}$ and inputting the Block Protect command performs block protection. The first cycle of the command sequence is the Setup command. In the second cycle, the Block Protect command is input, in which a block address and $A1 = V_{IH}$ and $A0 = A6 = V_{IL}$ are input. At this time, the device writes to the block protector circuit. Until write is complete, there must be a wait of t_{PPLH} but the device need not be controlled during this time. In the third cycle, the Verify Block Protect command is input. This command verifies write to the block protector circuit. Read is performed in the fourth cycle. If the protection operation is complete, 01H is output. If other than 01H is output, write is not complete; thus, input the Block Protect command again. Canceling VID to $\overline{\text{RESET}}$ exits this mode.

Temporary Block Unprotection

The TC58VSF2580/2581AASB has a temporary block unprotection feature which disables block protection for all protected blocks. Unprotection is enabled by applying VID to the $\overline{\text{RESET}}$ pin. Now Write and Erase operations can be performed on all blocks except the boot blocks which have been protected by the Boot Block Protect operation. The device returns to its previous state when VID is removed from the $\overline{\text{RESET}}$ pin. That is, previously protected blocks will be protected again.

Verify Block Protect

The Verify Block Protect command is used to ascertain whether a block is protected or unprotected. This mode is set by setting $A0$, $A6$ and the block address $A19 \sim A12$ to V_{IL} and setting $A1$ to V_{IH} . This command should be input before a Read operation is performed. 0001H is output if the block is protected and 0000H is output if the block is unprotected. In Byte Mode $DQ8$ to $DQ15$ are in High-Impedance state. Block protection verification can also be carried out using a software command.

Boot Block Protection

Boot block protection temporarily protects certain boot blocks using a method different from ordinary block protection. Neither VID nor a command sequence is required. Protection is performed simply by inputting V_{IL} on $\overline{\text{WP/ACC}}$. The target blocks are the two pairs of boot blocks. The top boot blocks are $BA69$ and $BA70$; the bottom boot blocks are $BA0$ and $BA1$. Inputting V_{IH} on $\overline{\text{WP/ACC}}$ releases the mode. From now on, if it is necessary to protect these blocks, the ordinary Block Protection Mode must be used.

Hidden ROM Area

The TH50VSF2580/2581AASB features a 64-Kbyte hidden ROM area which is separate from the memory cells. The area consists of one block. Data Read, Write and Protect can be performed on this block. Because Protect cannot be released, once the block is protected, data in the block cannot be overwritten.

The hidden ROM area is located in the address space indicated in the HIDDEN ROM AREA ADDRESS TABLE. To access the Hidden ROM area, input a Hidden ROM Mode Entry command. The device now enters Hidden ROM Mode, allowing Read, Write, Erase and Block Protect to be executed. Write and Erase operations are the same as auto operations except that the device is in Hidden ROM Mode. However, regarding write operation, Acceleration mode can not be performed during Hidden ROM mode. To protect the hidden ROM area, use the block protection function. The operation of Block Protect here is the same as a normal Block Protect except that V_{IH} rather than V_{ID} is input to \overline{RESET} . Once the block has been protected, protection cannot be released, even using the temporary block unprotection function. Use Block Protect carefully. Note that in Hidden ROM Mode, simultaneous operation cannot be performed. Therefore, do not attempt to access areas other than the hidden ROM area.

To exit Hidden ROM Mode, use the Hidden ROM Mode Exit command. This will return the device to Read Mode.

HIDDEN ROM AREA ADDRESS TABLE

| TYPE | BOOT BLOCK ARCHITECTURE | BYTE MODE | | WORD MODE | |
|-----------------|-------------------------|-------------------|-----------|------------------|-----------|
| | | ADDRESS RANGE | SIZE | ADDRESS RANGE | SIZE |
| TH50VSF2580AASB | TOP BOOT BLOCK | 3F0000H~3FFFFFFH | 64 Kbytes | 1F8000H~1FFFFFFH | 32 Kwords |
| TH50VSF2581AASB | BOTTOM BOOT BLOCK | 000000H~00FFFFFFH | 64 Kbytes | 000000H~007FFFFH | 32 Kwords |

COMMON FLASH MEMORY INTERFACE (CFI)

The TH50VSF2520/2581AASB conforms to the CFI specifications. To read information from the device, input the Query command followed by the address. In Word Mode DQ8~DQ15 all output 0s. To exit this mode, input the Reset command.

CFI CODE TABLE

| ADDRESS A6~A0 | DATA DQ15~DQ0 | DESCRIPTION |
|-------------------|-------------------------|--|
| 10H 11H 12H | 0051H 0052H 0059H | ASCII string "QRY" |
| 13H 14H | 0002H 0000H | Primary OEM command set 2: AMD/FJ standard type |
| 15H 16H | 0040H 0000H | Address for primary extended table |
| 17H 18H | 0000H 0000H | Alternate OEM command set 0: none exists |
| 19H 1AH | 0000H 0000H | Address for alternate OEM extended table |
| 1BH | 0027H | V _{DD} (min) (Write/Erase) DQ7~DQ4: 1 V DQ3~DQ0: 100 mV |
| 1CH | 0036H | V _{DD} (max) (Write/Erase) DQ7~DQ4: 1 V DQ3~DQ0: 100 mV |
| 1DH | 0000H | V _{PP} (min) voltage |
| 1EH | 0000H | V _{PP} (max) voltage |
| 1FH | 0004H | Typical time-out per single byte/word write (2 ^N μs) |
| 20H | 0000H | Typical time-out for minimum size buffer write (2 ^N μs) |
| 21H | 000AH | Typical time-out per individual block erase (2 ^N ms) |
| 22H | 0000H | Typical time-out for full chip erase (2 ^N ms) |
| 23H | 0005H | Maximum time-out for byte/word write (2 ^N times typical) |
| 24H | 0000H | Maximum time-out for buffer write (2 ^N times typical) |
| 25H | 0004H | Maximum time-out per individual block erase (2 ^N times typical) |
| 26H | 0000H | Maximum time-out for full chip erase (2 ^N times typical) |
| 27H | 0016H | Device Size (2 ^N byte) |
| 28H 29H | 0002H 0000H | Flash device interface description 2: ×8/×16 |
| 2AH 2BH | 0000H 0000H | Maximum number of bytes in multi-byte write (2 ^N) |

| ADDRESS A6~A0 | DATA DQ15~DQ0 | DESCRIPTION |
|---------------|---------------|--|
| 2CH | 0002H | Number of erase block regions within device |
| 2DH | 0007H | Erase Block Region 1 information Bits 0~15: y = block number Bits 16~31: z = block size (z × 256 bytes) |
| 2EH | 0000H | |
| 2FH | 0020H | |
| 30H | 0000H | |
| 31H | 003EH | Erase Block Region 2 information |
| 32H | 0000H | |
| 33H | 0000H | |
| 34H | 0001H | |
| 40H | 0050H | ASCII string "PRI" |
| 41H | 0052H | |
| 42H | 0049H | |
| 43H | 0031H | Major version number, ASCII |
| 44H | 0031H | Minor version number, ASCII |
| 45H | 0000H | Address-Sensitive Unlock 0: Required 1: Not required |
| 46H | 0002H | Erase Suspend 0: Not supported 1: For Read-only 2: For Read & Write |
| 47H | 0001H | Block Protect 0: Not supported X: Number of blocks per group |
| 48H | 0001H | Block Temporary Unprotect 0: Not supported 1: Supported |
| 49H | 0004H | Block Protect/Unprotect scheme |
| 4AH | 0001H | Simultaneous operation 0: Not supported 1: Supported |
| 4BH | 0000H | Burst Mode 0: Not supported |
| 4CH | 0000H | Page Mode 0: Not supported |
| 4DH | 0085H | V _{ACC} (min) voltage DQ7~DQ4: 1 V DQ3~DQ0: 100 mV |
| 4EH | 0095H | V _{ACC} (max) voltage DQ7~DQ4: 1 V DQ3~DQ0: 100 mV |
| 4FH | 000XH | Top/Bottom Boot Block Flag 2: TH50VSF2580AASB 3: TH50VSF2581AASB |
| 50H | 0001H | Program suspend 0: Not supported 1: Supported |

HARDWARE SEQUENCE FLAGS FOR FLASH MEMORY

The TH50VSF2580/2581AASB has a Hardware Sequence flag which allows the device status to be determined during an auto mode operation. The output data is read out using the same timing as that used when $\overline{CE\overline{F}} = \overline{OE} = V_{IL}$ in Read Mode. The $\overline{RY/B\overline{Y}}$ output can be either High or Low.

The device re-enters Read Mode automatically after an auto mode operation has been completed successfully. The Hardware Sequence flag is read to determine the device status and the result of the operation is verified by comparing the read-out data with the original data.

DQ7 (DATA polling)

During an Auto-Program or auto-erase operation, the device status can be determined using the data polling function. \overline{DATA} polling begins on the rising edge of \overline{WE} in the last bus cycle. In an Auto-Program operation, DQ7 outputs inverted data during the programming operation and outputs actual data after programming has finished. In an auto-erase operation, DQ7 outputs 0 during the Erase operation and outputs 1 when the Erase operation has finished. If an Auto-Program or auto-erase operation fails, DQ7 simply outputs the data.

When the operation has finished, the address latch is reset. Data polling is asynchronous with the \overline{OE} signal.

DQ6 (Toggle bit 1)

The device status can be determined by the Toggle Bit function during an Auto-Program or auto-erase operation. The Toggle bit begins toggling on the rising edge of \overline{WE} in the last bus cycle. DQ6 alternately outputs a 0 or a 1 for each \overline{OE} access while $\overline{CE\overline{F}} = V_{IL}$ while the device is busy. When the internal operation has been completed, toggling stops and valid memory cell data can be read by subsequent reading. If the operation fails, the DQ6 output toggles.

If an attempt is made to execute an Auto Program operation on a protected block, DQ6 will toggle for around 3 μ s. It will then stop toggling. If an attempt is made to execute an auto erase operation on a protected block, DQ6 will toggle for around 100 μ s. It will then stop toggling. After toggling has stopped the device will return to Read Mode.

DQ5 (internal time-out)

If the internal timer times out during a Program or Erase operation, DQ5 outputs a 1. This indicates that the operation has not been completed within the allotted time.

Any attempt to program a 1 into a cell containing a 0 will fail (see Auto-Program Mode). In this case DQ5 outputs a 1. Either a hardware reset or a software Reset command is required to return the device to Read Mode.

DQ3 (Block Erase timer)

The Block Erase operation starts 50 μ s (the Erase Hold Time) after the rising edge of \overline{WE} in the last command cycle. DQ3 outputs a 0 for the duration of the Block Erase Hold Time and a 1 when the Block Erase operation starts. Additional Block Erase commands can only be accepted during the Block Erase Hold Time. Each Block Erase command input within the hold time resets the timer, allowing additional blocks to be marked for erasing. DQ3 outputs a 1 if the Program or Erase operation fails.

DQ2 (Toggle bit 2)

DQ2 is used to indicate which blocks have been selected for Auto Block Erase or to indicate whether the device is in Erase Suspend Mode.

If data is read continuously from the selected block during an Auto Block Erase, the DQ2 output will toggle. Now 1 will be output from non-selected blocks; thus, the selected block can be ascertained. If data is read continuously from the block selected for Auto Block Erase while the device is in Erase Suspend Mode, the DQ2 output will toggle. Because the DQ6 output is not toggling, it can be determined that the device is in Erase Suspend Mode. If data is read from the address to which data is being written during Erase Suspend in Programming Mode, DQ2 will output a 1.

RY/ \overline{BY} (READY/ \overline{BUSY})

The TH50VSF2580/2581AASB has a RY/ \overline{BY} signal to indicate the device status to the host processor. A 0 (Busy state) indicates that an Auto-Program or auto-erase operation is in progress. A 1 (Ready state) indicates that the operation has finished and that the device can now accept a new command. RY/ \overline{BY} outputs a 0 when an operation has failed.

RY/ \overline{BY} outputs a 0 after the rising edge of \overline{WE} in the last command cycle.

During an Auto Block Erase operation, commands other than Erase Suspend are ignored. RY/ \overline{BY} outputs a 1 during an Erase Suspend operation. The output buffer for the RY/ \overline{BY} pin is an open-drain type circuit, allowing a wired-OR connection. A pull-up resistor must be inserted between VCC and the RY/ \overline{BY} pin.

DATA PROTECTION

The TH50VSF2580/2581AASB includes a function which guards against malfunction or data corruption.

Protection against Program/Erase Caused by Low Supply Voltage

To prevent malfunction at power-on or power-down, the device will not accept commands while V_{CCf} is below V_{LKO} . In this state, command input is ignored.

If V_{CCf} drops below V_{LKO} during an Auto Operation, the device will terminate Auto-Program execution. In this case, Auto operation is not executed again when V_{CCf} return to recommended V_{CCf} voltage. Therefore, command need to be input to execute Auto operation again.

When $V_{CCf} > V_{LKO}$, make up countermeasure to be input accurately command in system side please.

Protection against Malfunction Caused by Glitches

To prevent malfunction during operation caused by noise from the system, the device will not accept pulses shorter than 3 ns(Typ.) input on \overline{WE} , \overline{CEf} or \overline{OE} . However, if a glitch exceeding 3 ns(Typ.) occurs and the glitch is input to the device malfunction may occur.

The device uses standard JEDEC commands. It is conceivable that, in extreme cases, system noise may be misinterpreted as part of a command sequence input and that the device will acknowledge it. Then, even if a proper command is input, the device may not operate. To avoid this possibility, clear the Command Register before command input. In an environment prone to system noise, Toshiba recommend input of a software or hardware reset before command input.

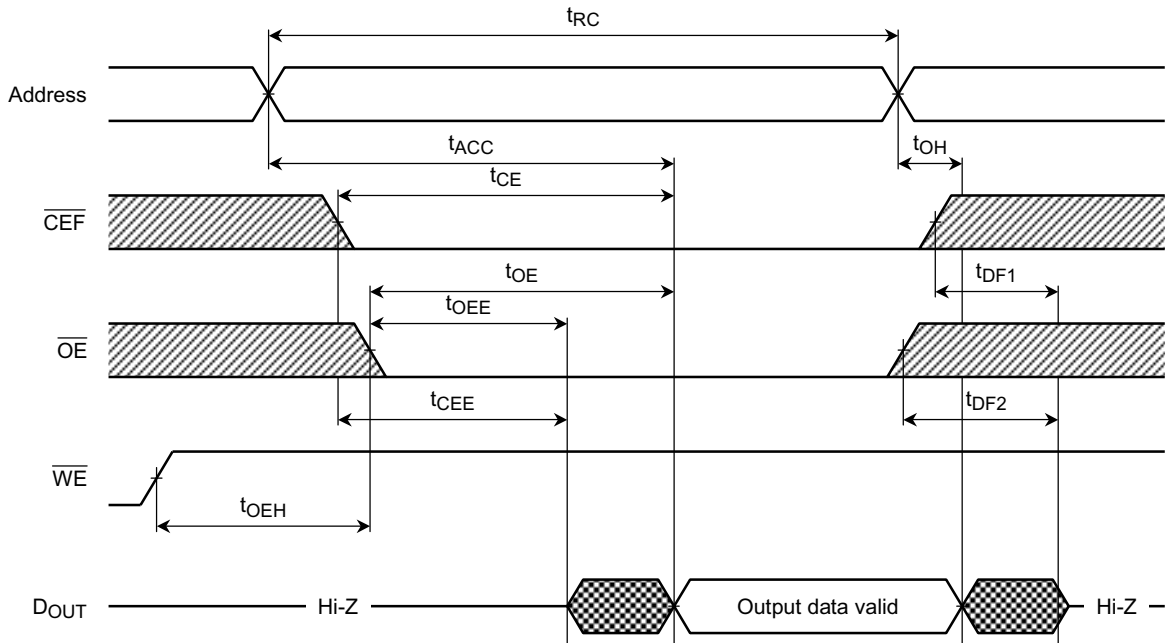
Protection against Malfunction at Power-on

To prevent damage to data caused by sudden noise at power-on, when power is turned on with $\overline{WE} = \overline{CEf} = V_{IL}$, the device does not latch the command on the first rising edge of \overline{WE} or \overline{CEf} . Instead, the device automatically Resets the Command Register and enters Read Mode.

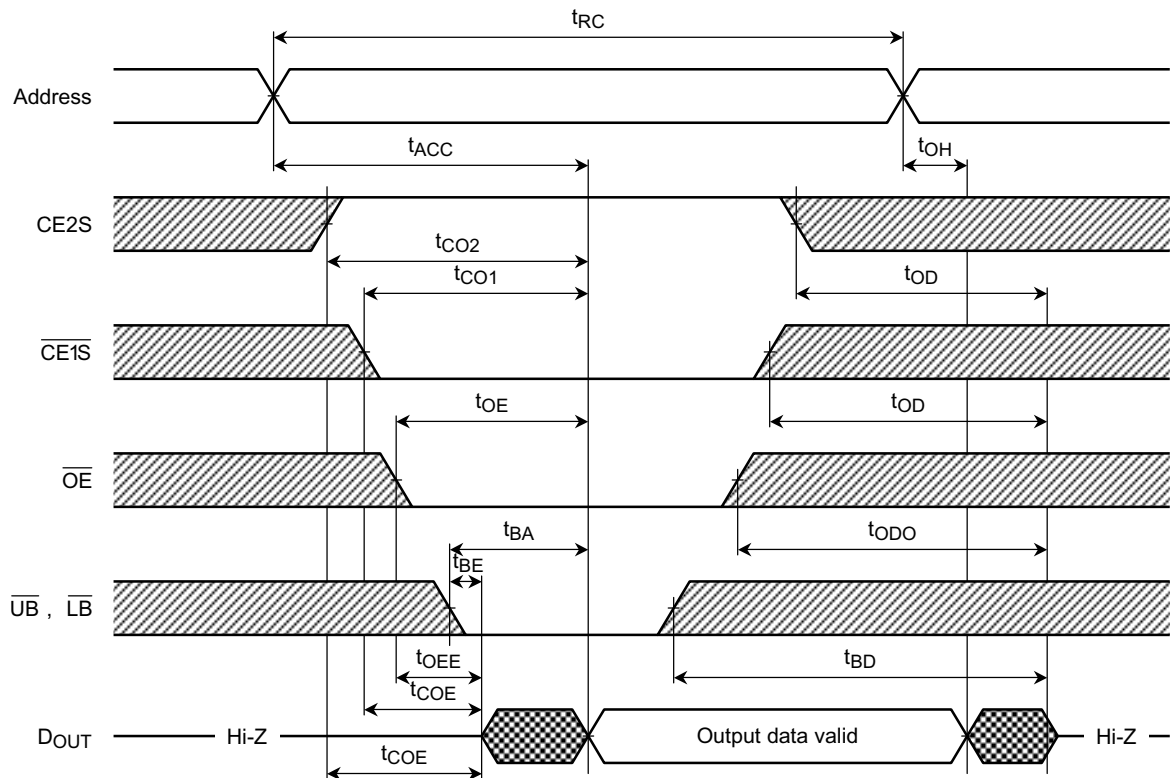
TIMING DIAGRAMS



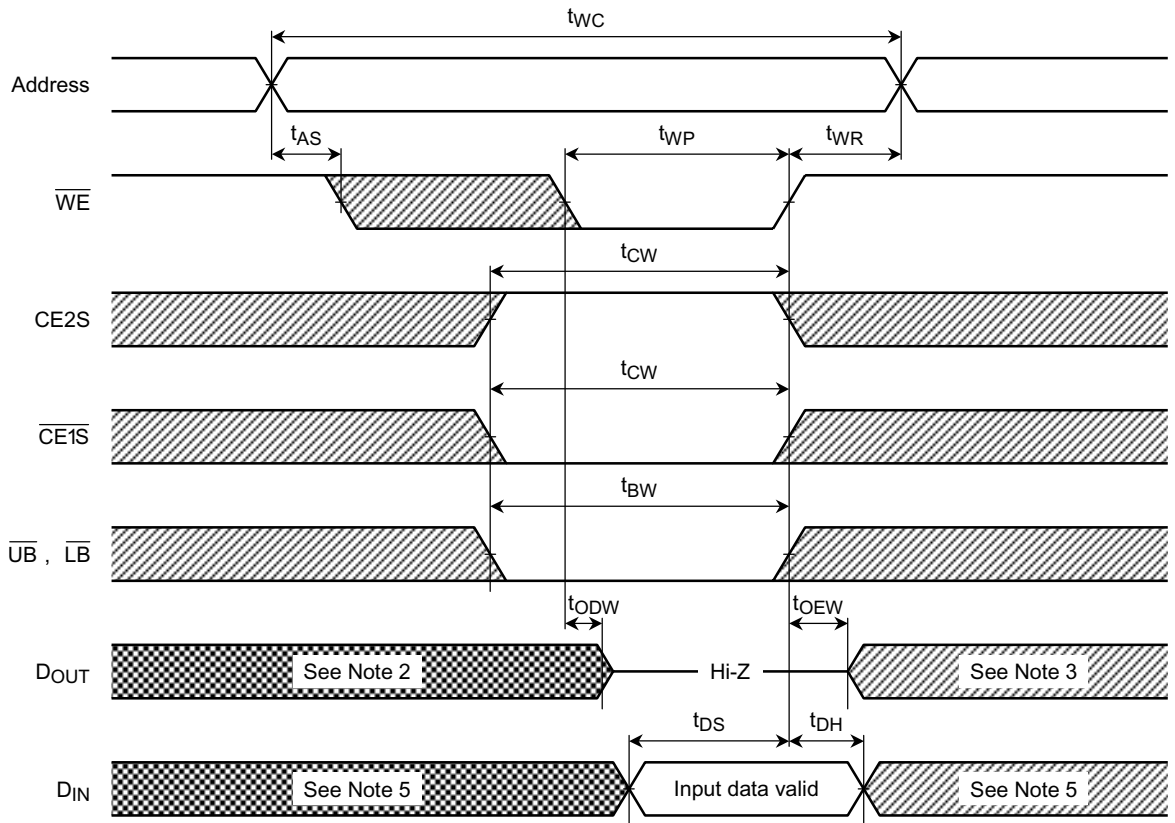
FLASH READ/ID READ OPERATION



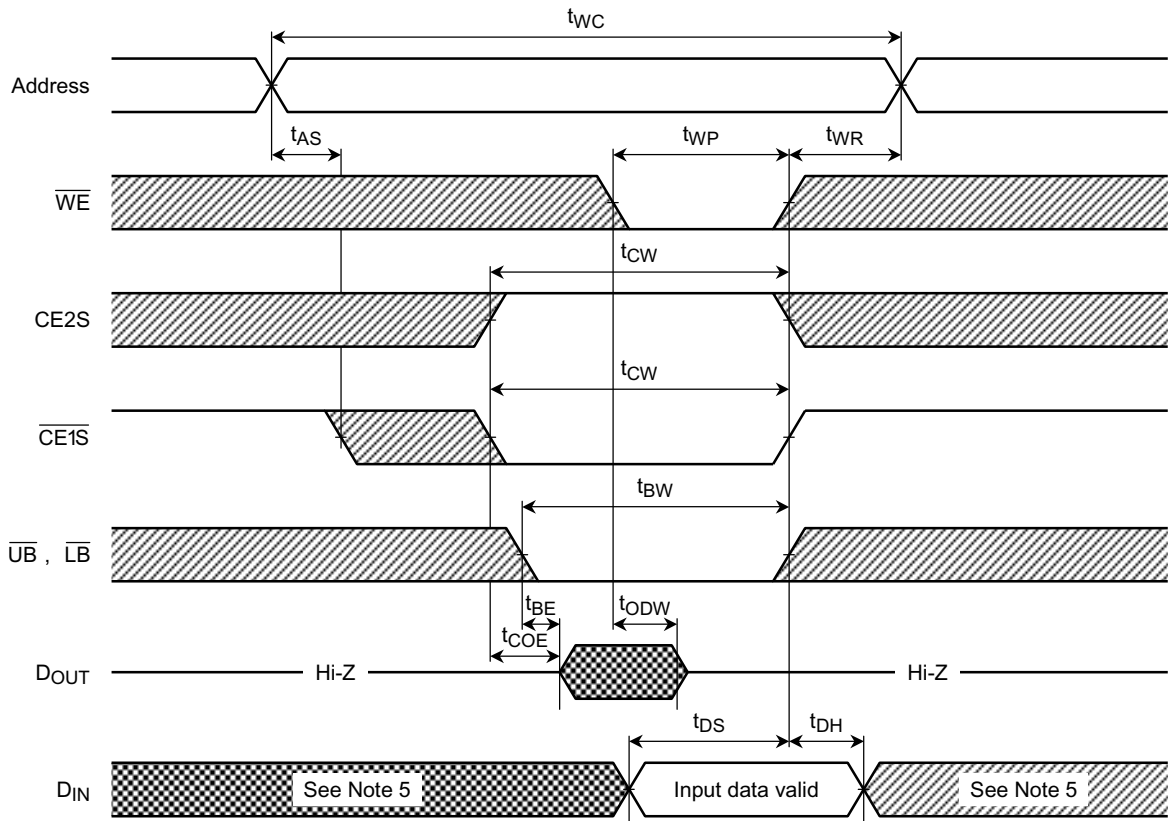
SRAM READ CYCLE (see Note 1)



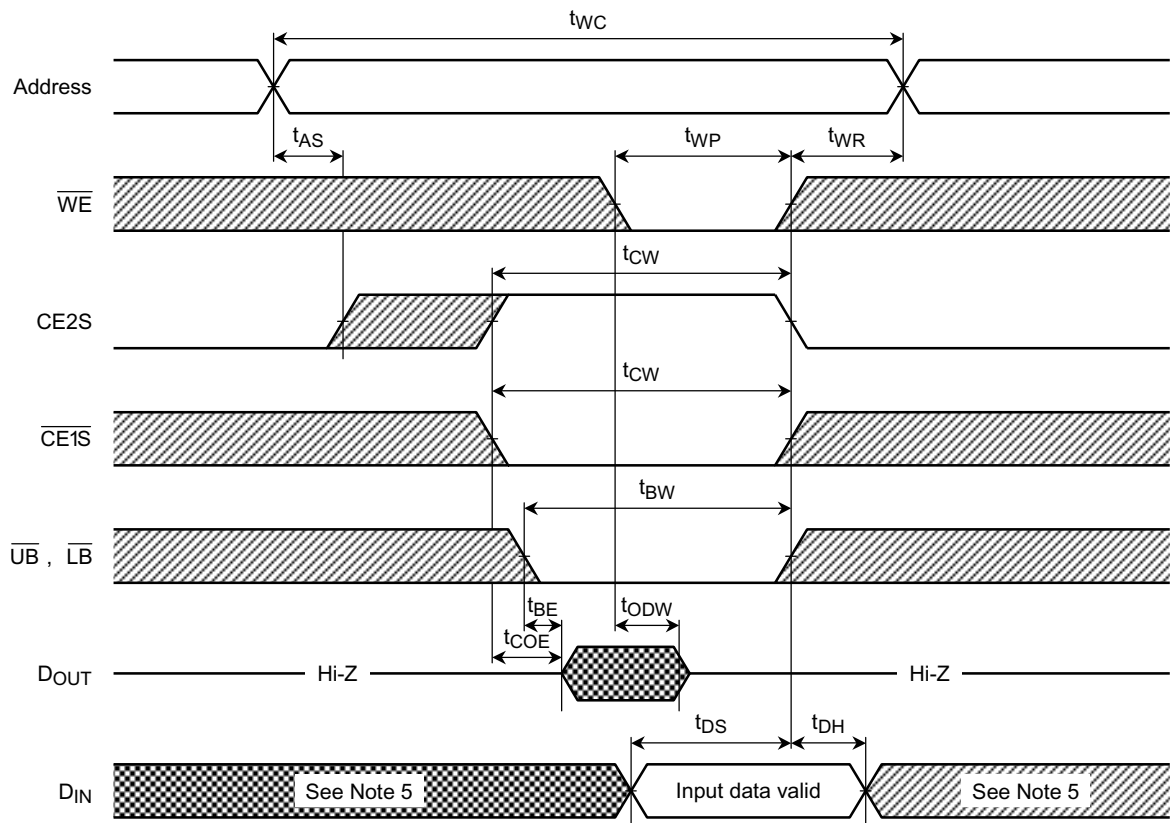
SRAM WRITE CYCLE 1 (\overline{WE} -CONTROLLED) (see Note 4)



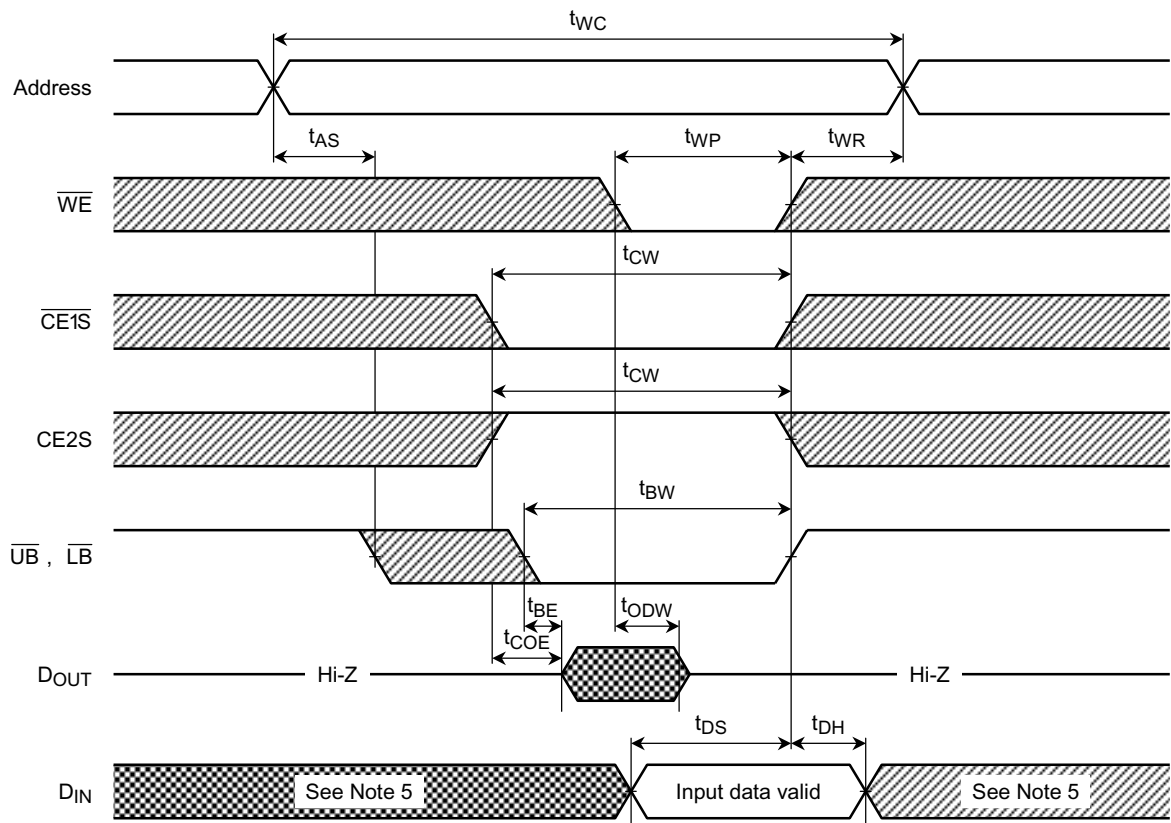
SRAM WRITE CYCLE 2 ($\overline{CE1S}$ -CONTROLLED) (see Note 4)



SRAM WRITE CYCLE 3 (CE2S-CONTROLLED) (see Note 4)



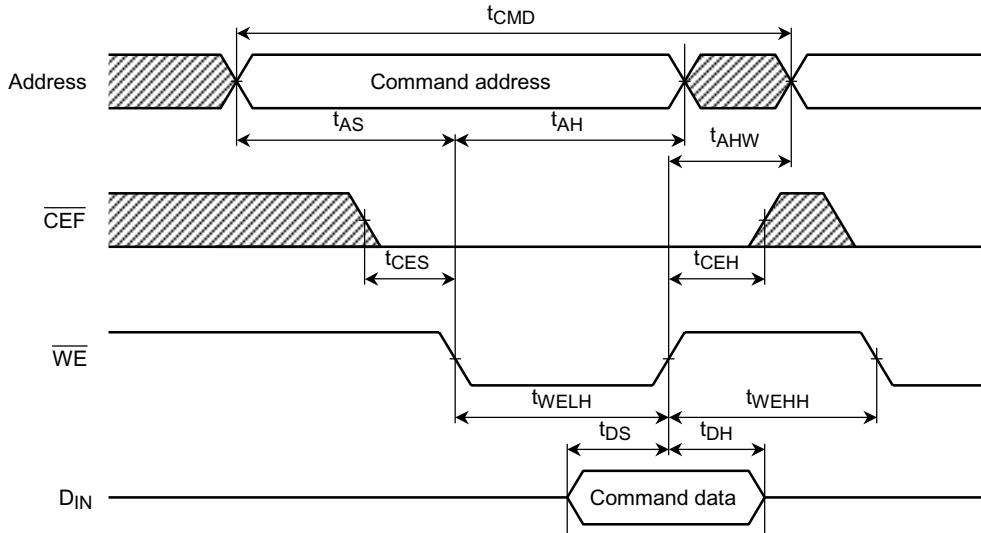
SRAM WRITE CYCLE 4 (\overline{UB} - and \overline{LB} -CONTROLLED) (see Note 4)



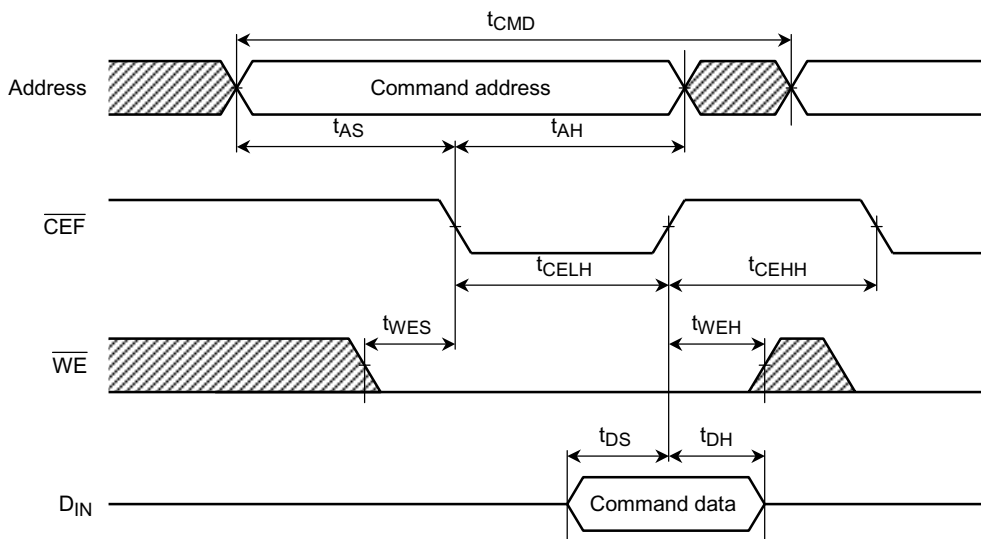
FLASH COMMAND WRITE OPERATION

This is the timing of the Command Write Operation. The timing which is described in the following pages is essentially the same as the timing shown on this page.

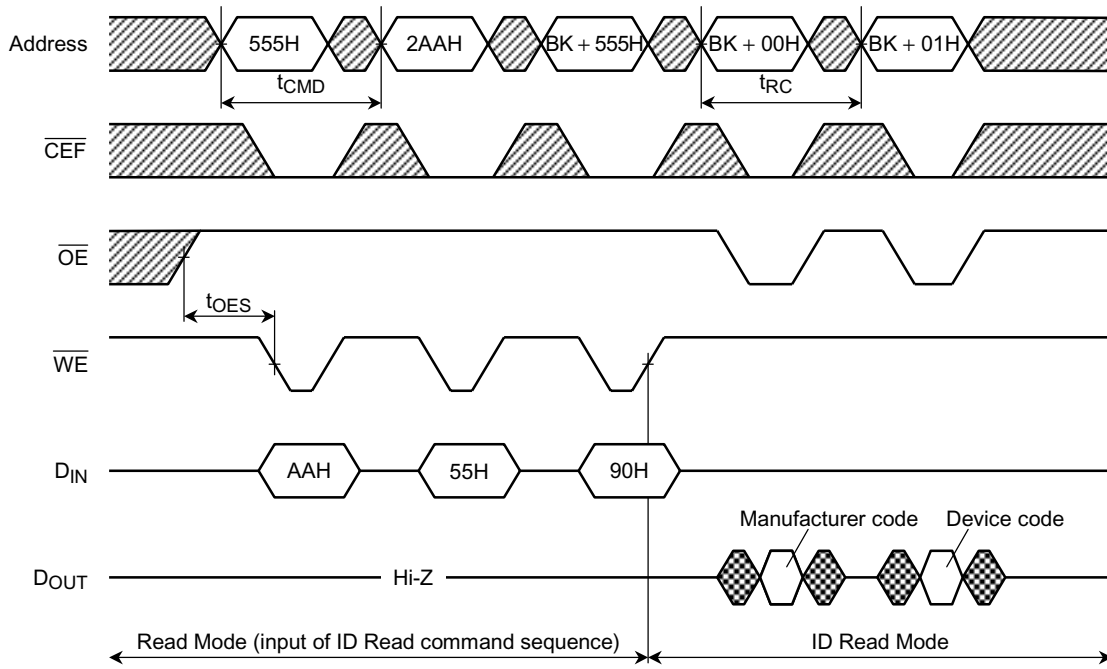
- \overline{WE} Control



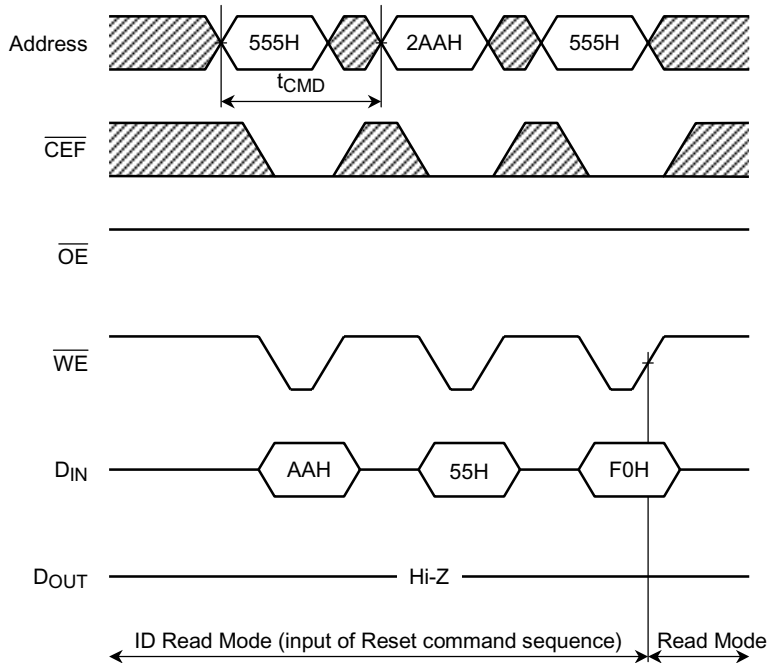
- \overline{CE} Control



FLASH ID READ OPERATION (Input command sequence)

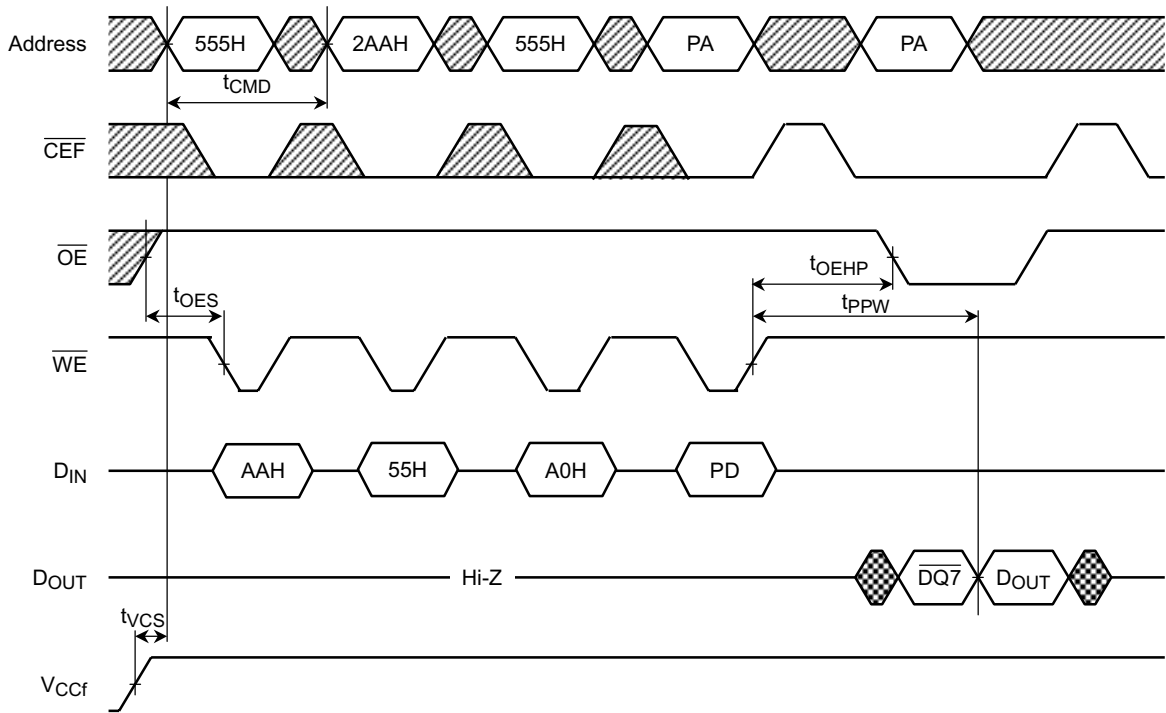


(Continued)



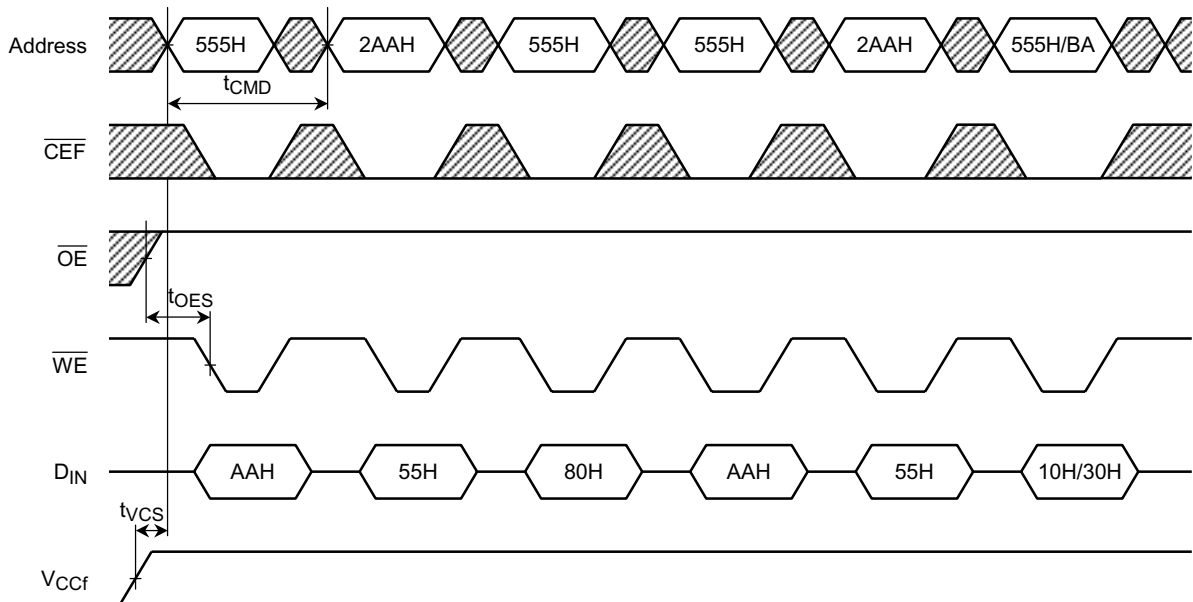
Note: Word Mode address shown.
BK: Bank address

FLASH AUTO-PROGRAM OPERATION (\overline{WE} -CONTROLLED)



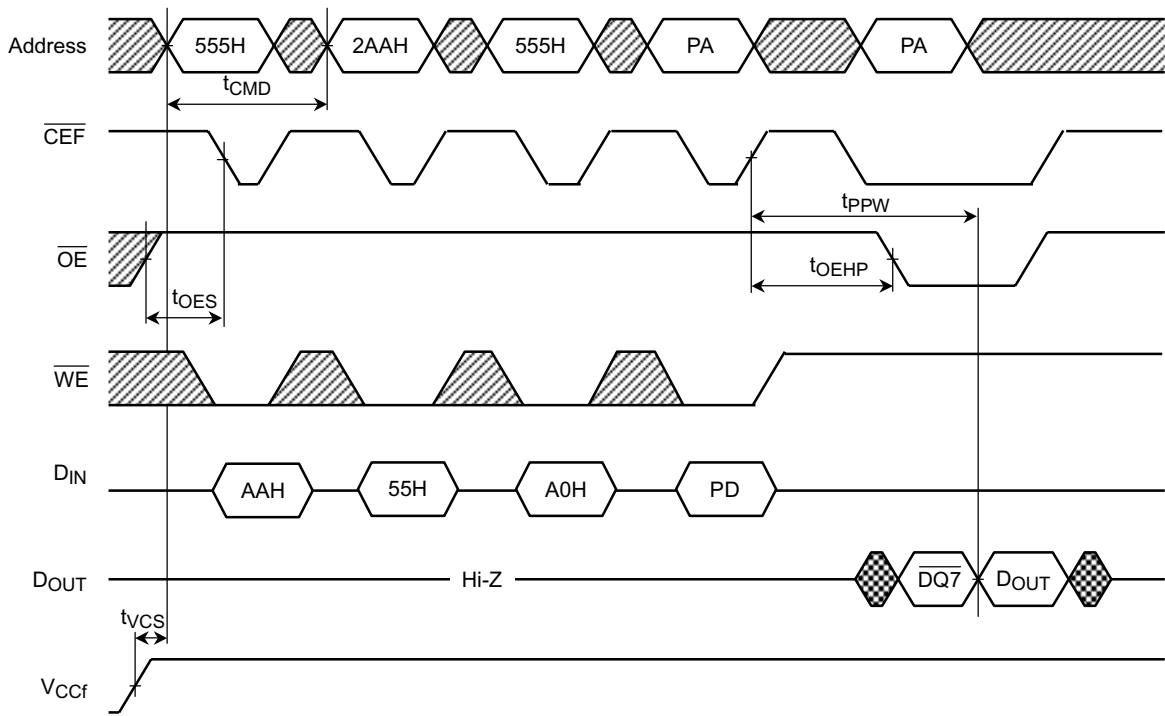
Note: Word Mode address shown.
 PA: Program address
 PD: Program data

FLASH AUTO CHIP ERASE / AUTO BLOCK ERASE OPERATION (\overline{WE} -CONTROLLED)



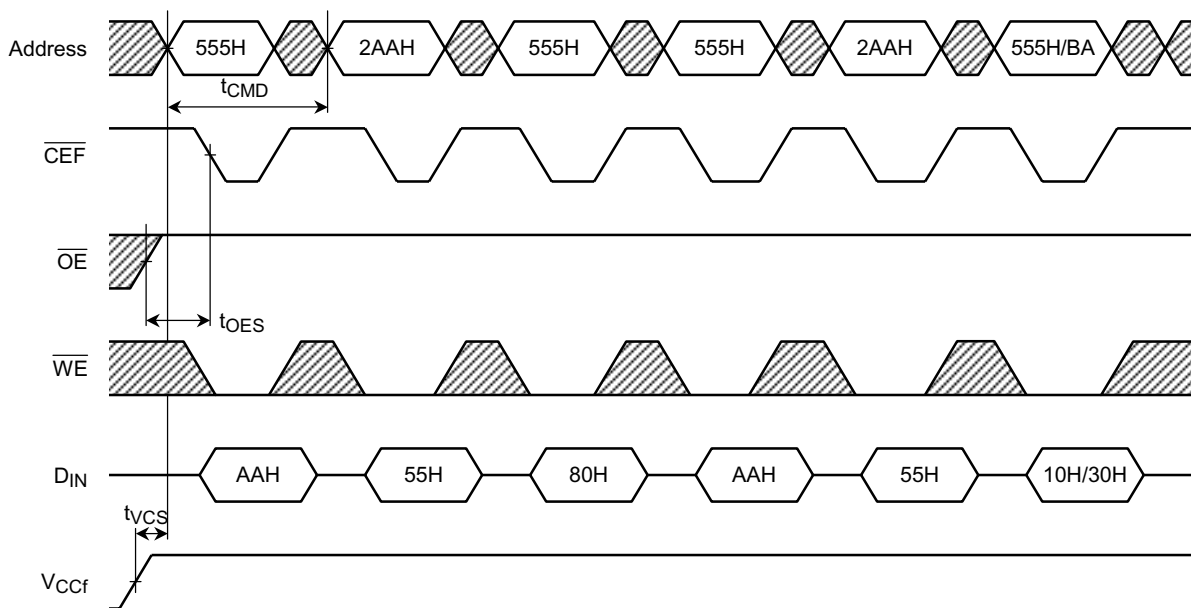
Note: Word Mode address shown.
 BA: Block address for Auto Block Erase operation

FLASH AUTO-PROGRAM OPERATION ($\overline{\text{CE}}\overline{\text{F}}$ -CONTROLLED)



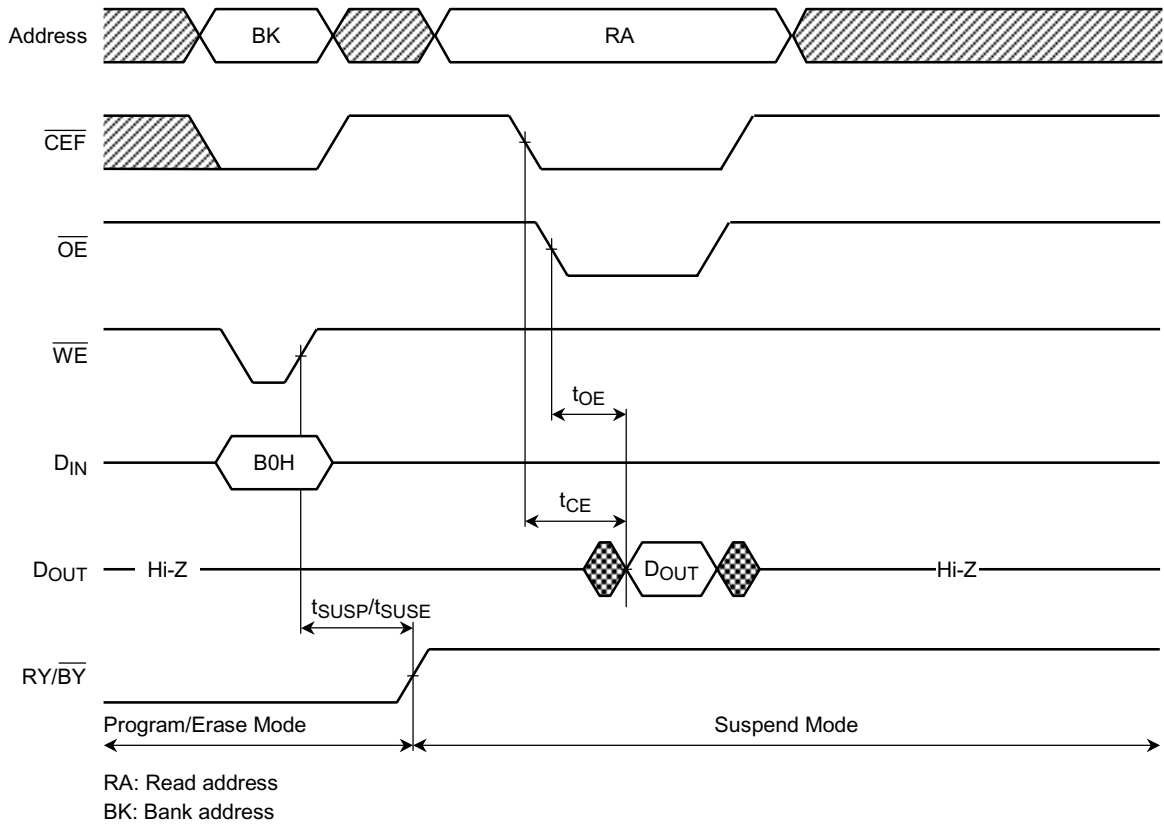
Note: Word Mode address shown.
 PA: Program address
 PD: Program data

FLASH AUTO CHIP ERASE / AUTO BLOCK ERASE OPERATION ($\overline{\text{CE}}\overline{\text{F}}$ -CONTROLLED)

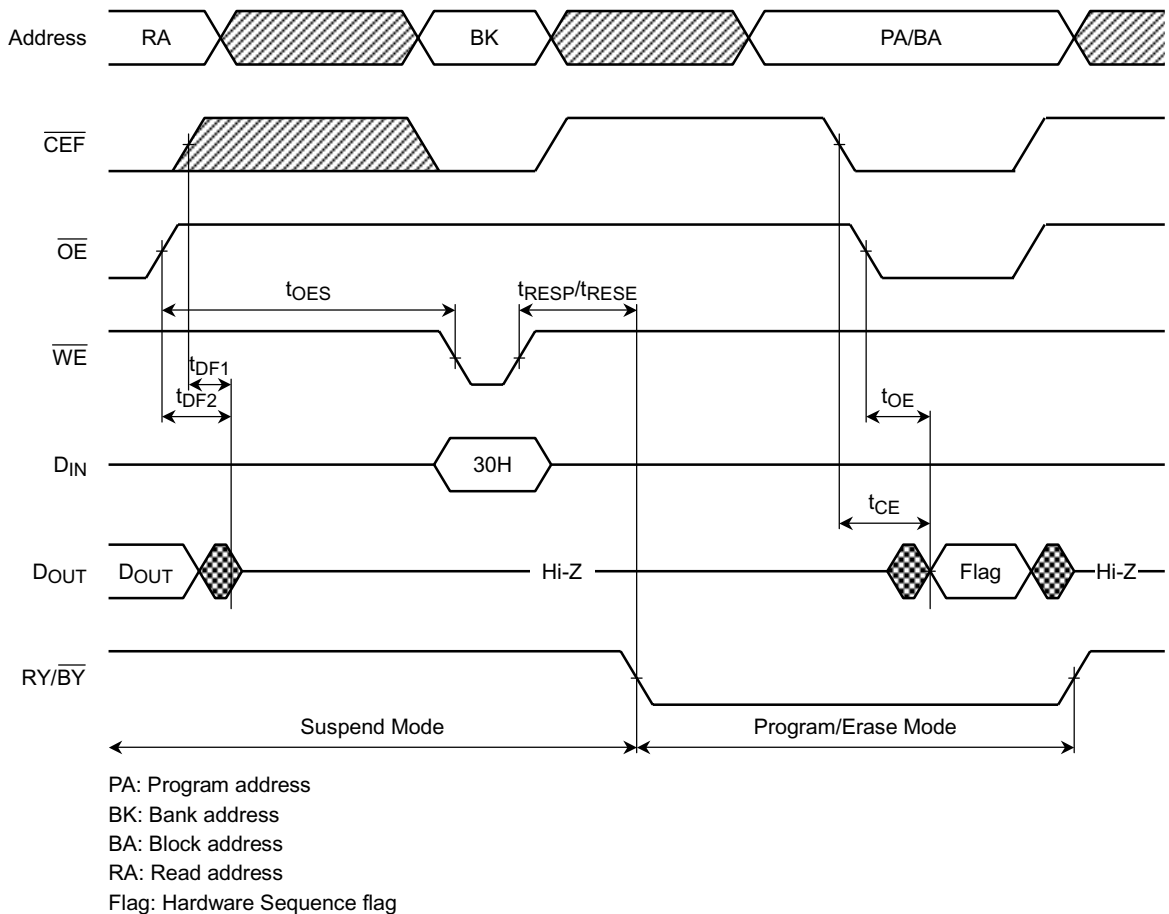


Note: Word Mode address shown.
 BA: Block address for Auto Block Erase operation

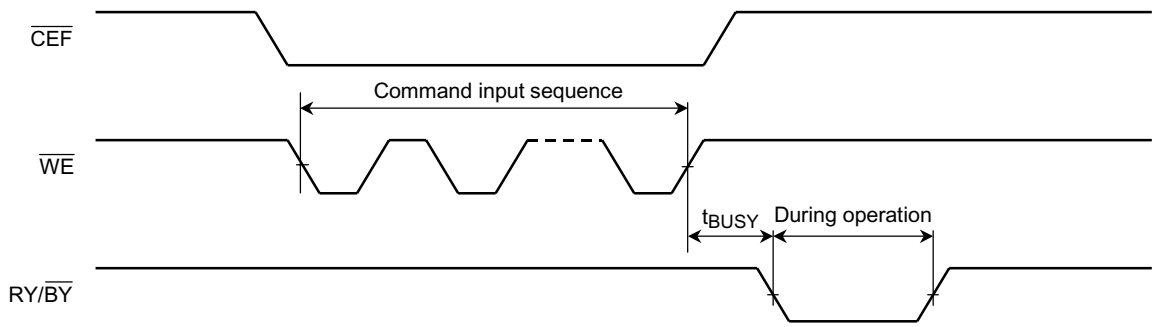
FLASH PROGRAM/ERASE SUSPEND OPERATION



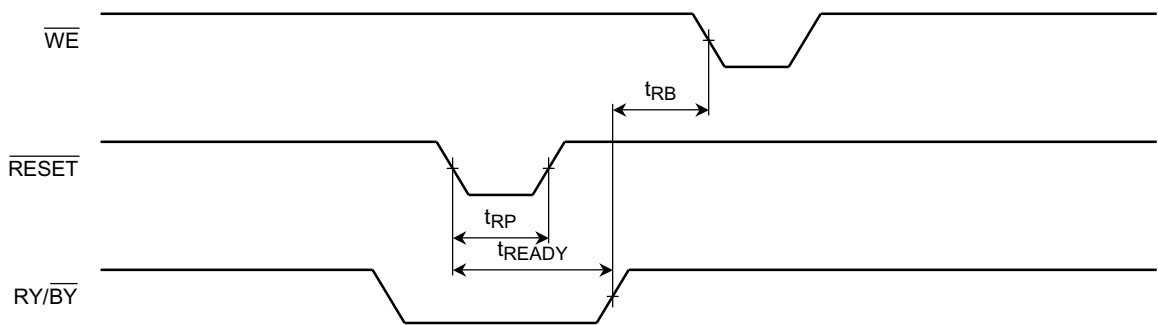
FLASH PROGRAM/ERASE RESUME OPERATION



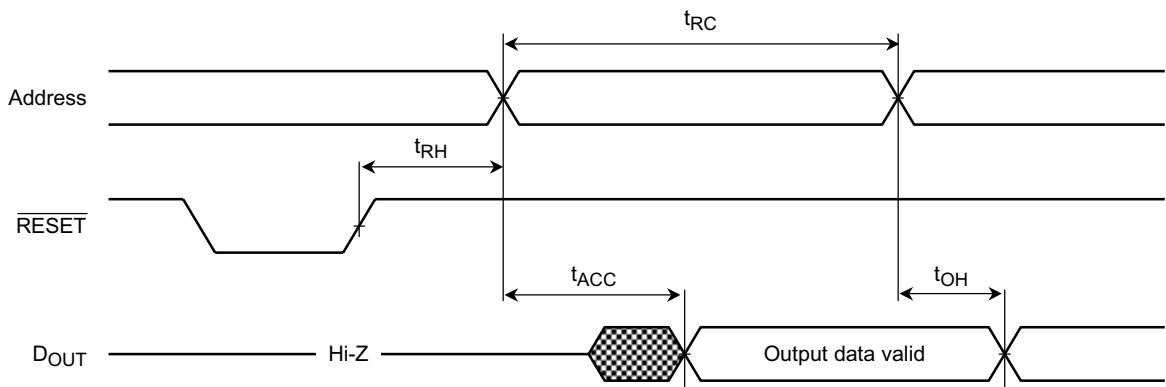
FLASH RY/ $\overline{\text{BY}}$ DURING AUTO-PROGRAM/ERASE OPERATION



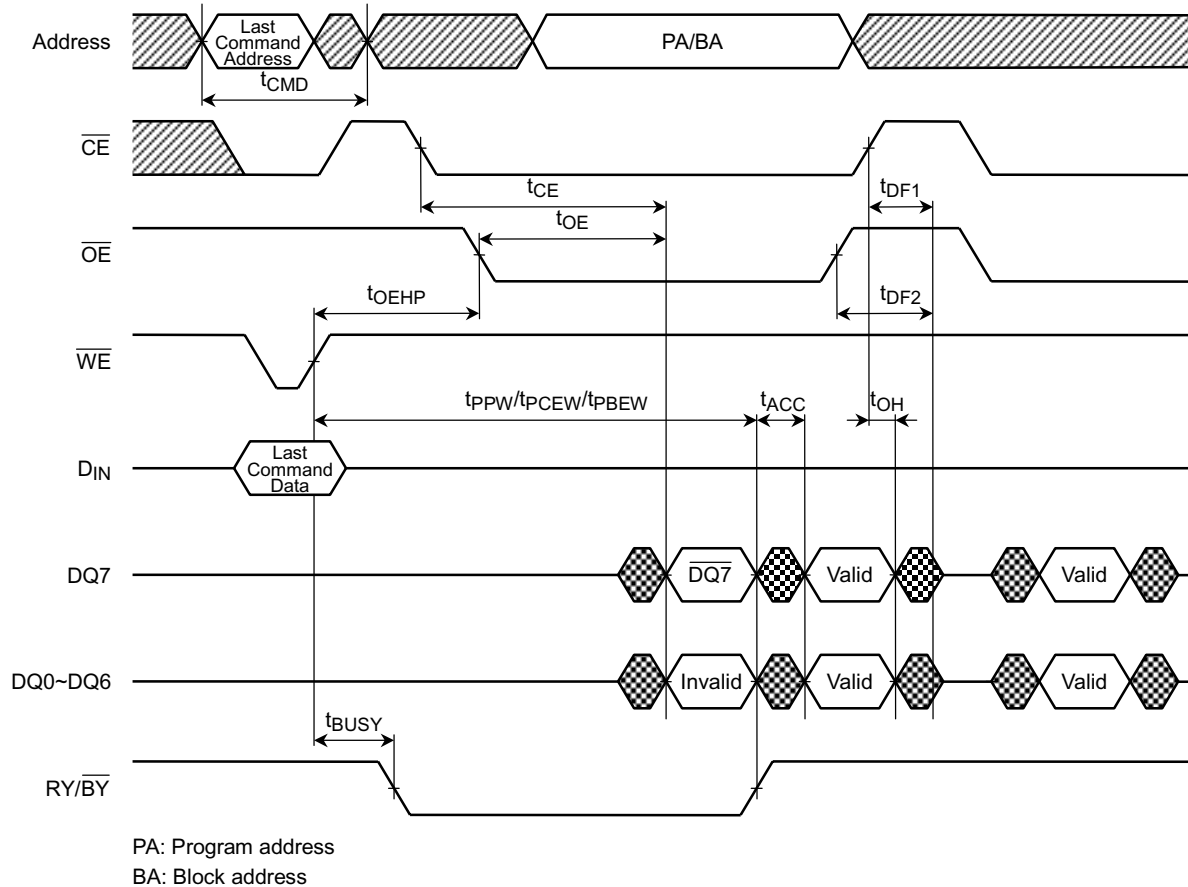
FLASH HARDWARE RESET OPERATION



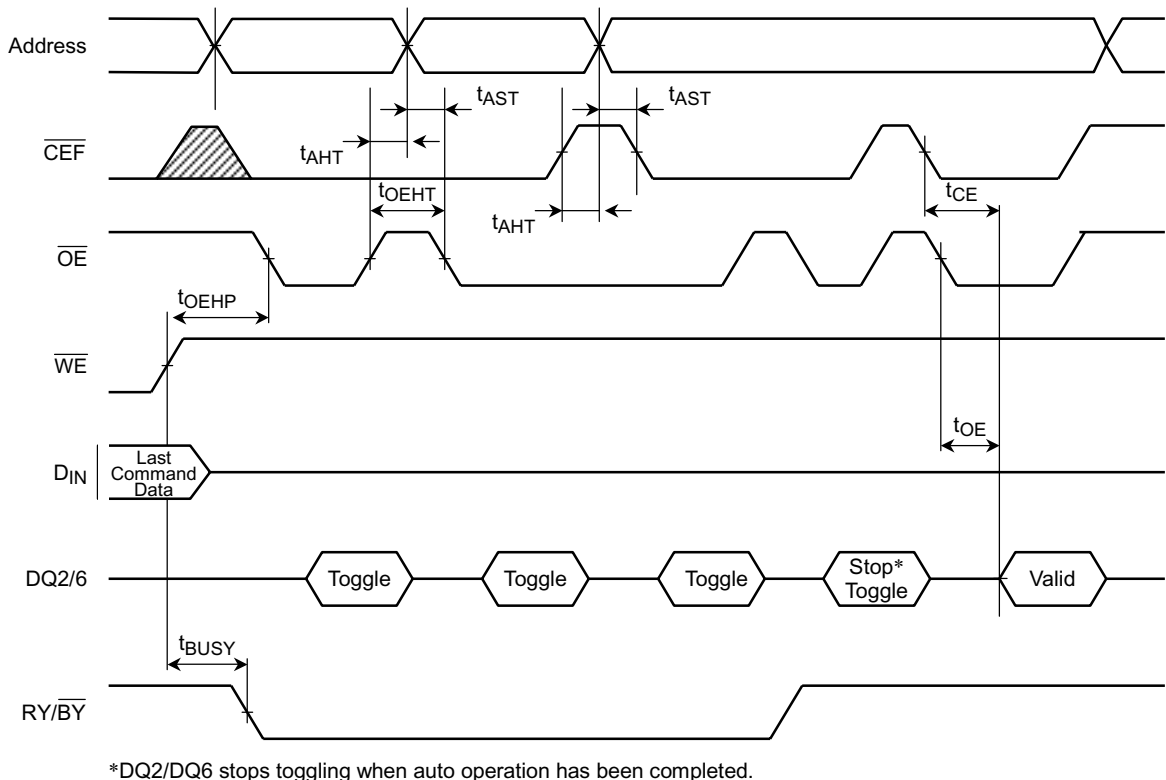
FLASH READ AFTER $\overline{\text{RESET}}$



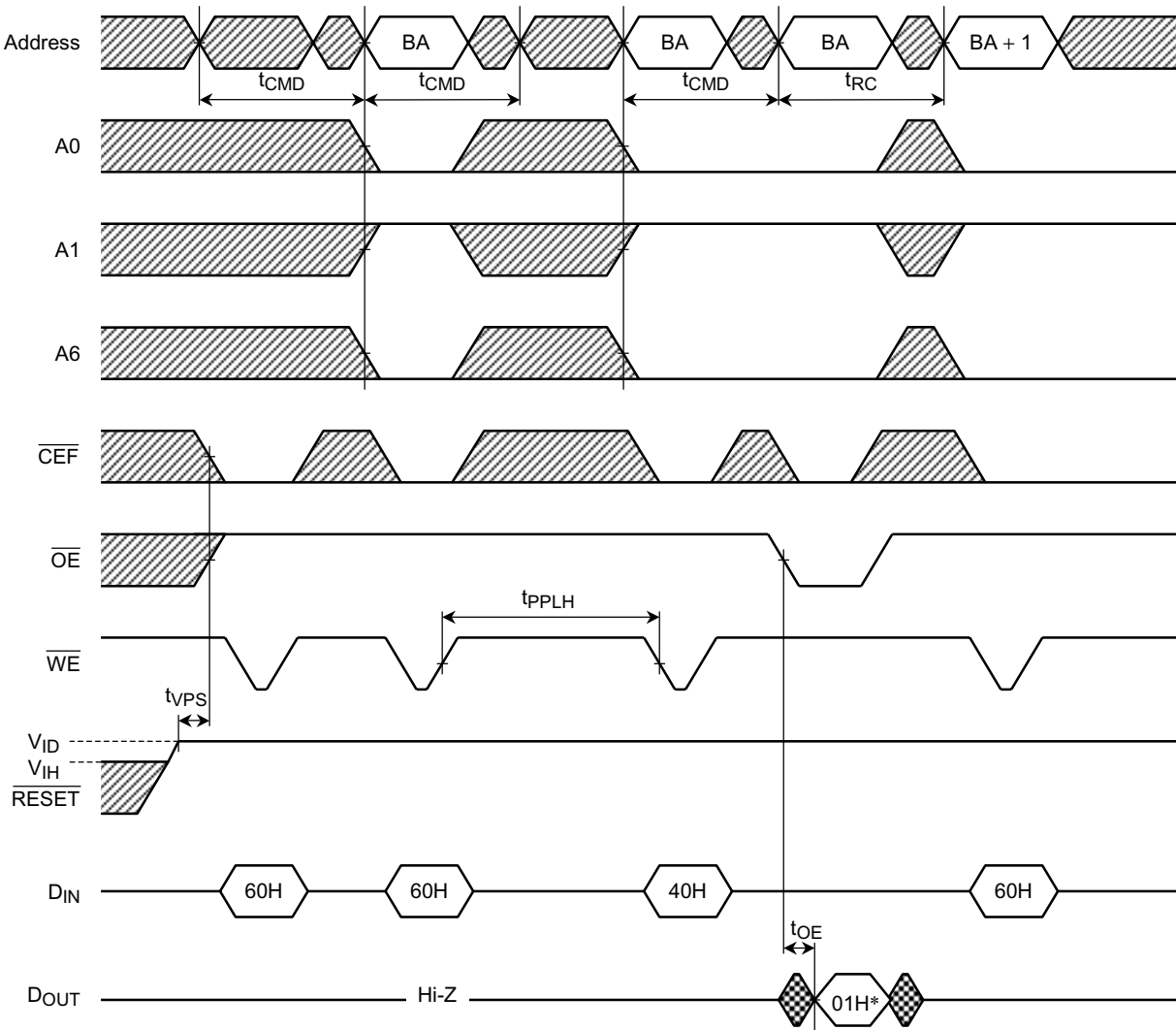
FLASH HARDWARE SEQUENCE FLAG ($\overline{\text{DATA}}$ Polling)



FLASH HARDWARE SEQUENCE FLAG (Toggle bit)

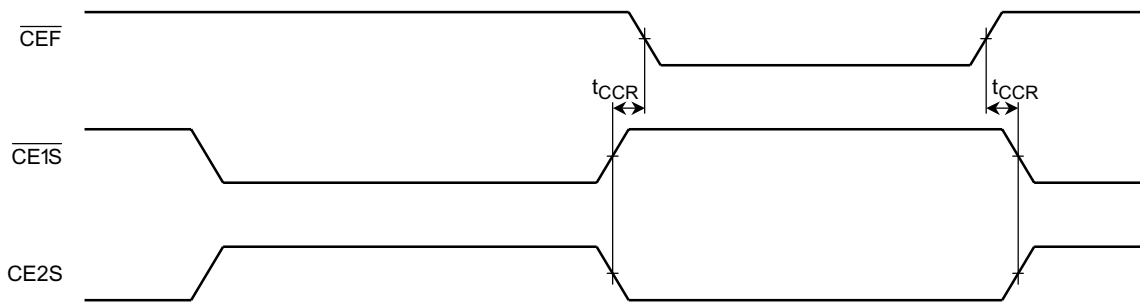


FLASH BLOCK PROTECT OPERATION



BA: Block address
 BA + 1: Address of next block
 *: 01H indicates that block is protected.

TIMING FOR SWITCHING BETWEEN FLASH AND SRAM MODES



Notes:

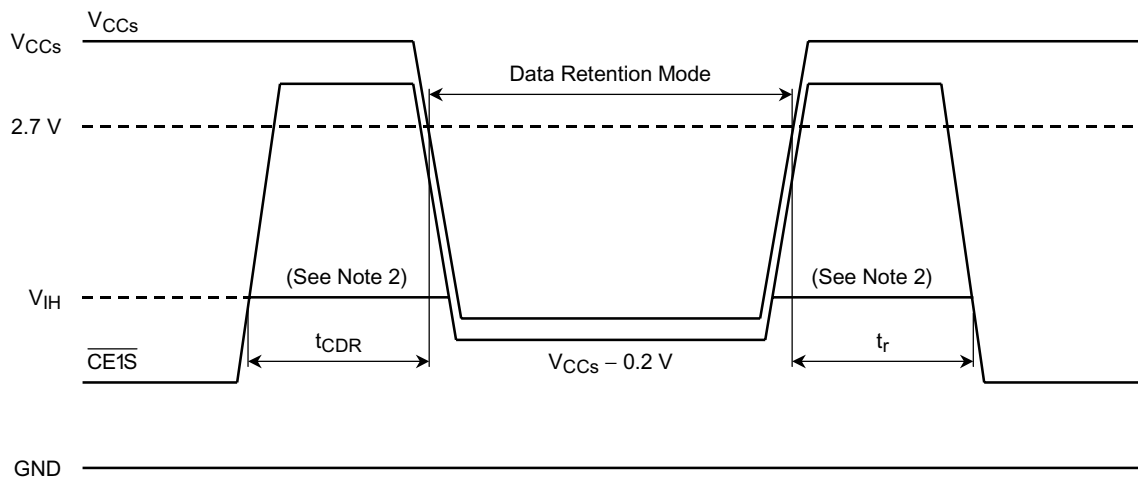
- (1) \overline{WE} remains High during a Read cycle.
- (2) If $\overline{CE1\overline{S}}$ goes Low (or $CE2\overline{S}$ goes High) at the same time as or after \overline{WE} goes Low, the outputs will remain High-Impedance.
- (3) If $\overline{CE1\overline{S}}$ goes High (or $CE2\overline{S}$ goes Low) at the same time as or before \overline{WE} goes High, the outputs will remain High-Impedance.
- (4) If \overline{OE} is High during a Write cycle, the outputs will remain High-Impedance.
- (5) Since I/O pins may be in Output state at this point, do not attempt to apply input signals to them.
- (6) DOUT6 stops toggling when the last command has been completed.

SRAM DATA RETENTION CHARACTERISTICS (Ta = -40°~85°C)

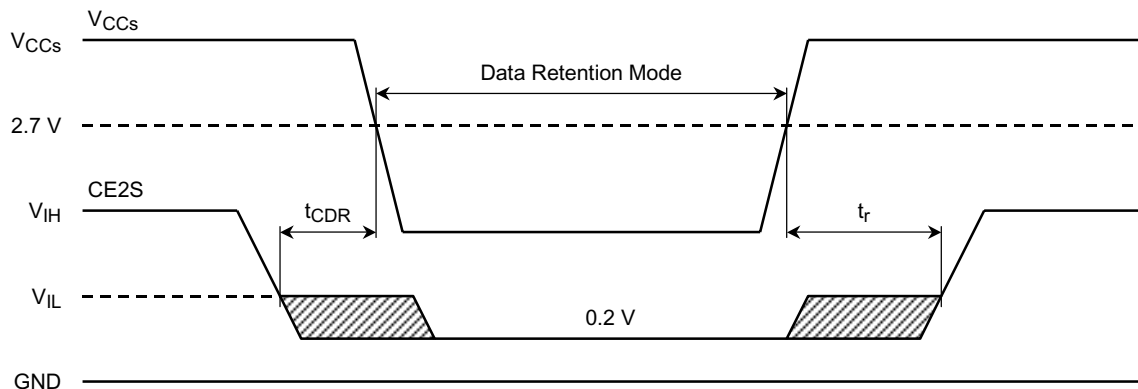
| SYMBOL | PARAMETER | MIN | TYP. | MAX | UNIT |
|-------------------|---|--------------------------------|------|-----|------|
| V _{DH} | Data Retention Supply Voltage for SRAM | 1.5 | — | 3.6 | V |
| I _{CCS4} | SRAM Standby Current | V _{DH} = 3.0 V | — | 5 | μA |
| | | V _{DH} = 3.6 V | — | 7 | |
| t _{CDR} | Chip-Deselect-to-Data-Retention-Mode Time | 0 | — | — | ns |
| t _r | Recovery Time | t _{RC} ⁽¹⁾ | — | — | ns |

(1) Read cycle time

CE1S-CONTROLLED DATA RETENTION MODE (see Note 1)



CE2S-CONTROLLED DATA RETENTION MODE (see Note 3)

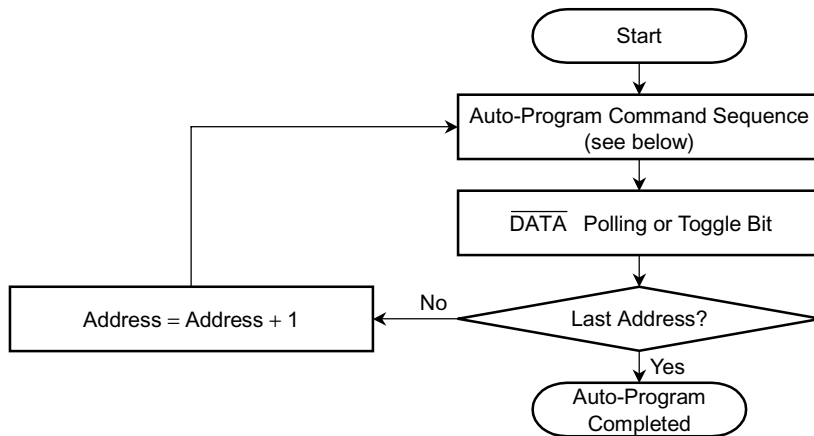


Notes:

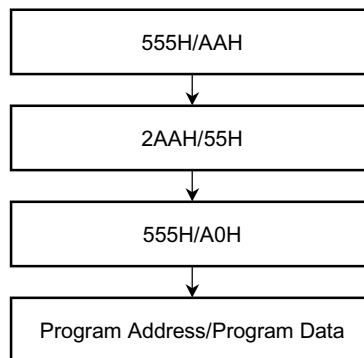
- (1) In $\overline{\text{CE1S}}$ -Controlled Data Retention Mode the device enters Minimum Standby Current Mode when $\overline{\text{CE2S}} \leq 0.2 \text{ V}$ or $\overline{\text{CE2S}} \geq V_{\text{CCS}} - 0.2 \text{ V}$.
- (2) When $\overline{\text{CE1S}}$ is at V_{IH} (2.2 V), the SRAM standby current is the same as I_{CCS3} during the transition of V_{CCS} from 3.6 V to 2.4 V.
- (3) In CE2S-Controlled Data Retention Mode the device enters Minimum Standby Current Mode when $\text{CE2S} \leq 0.2 \text{ V}$.

FLOWCHARTS OF FLASH MEMORY OPERATIONS

Auto-Program

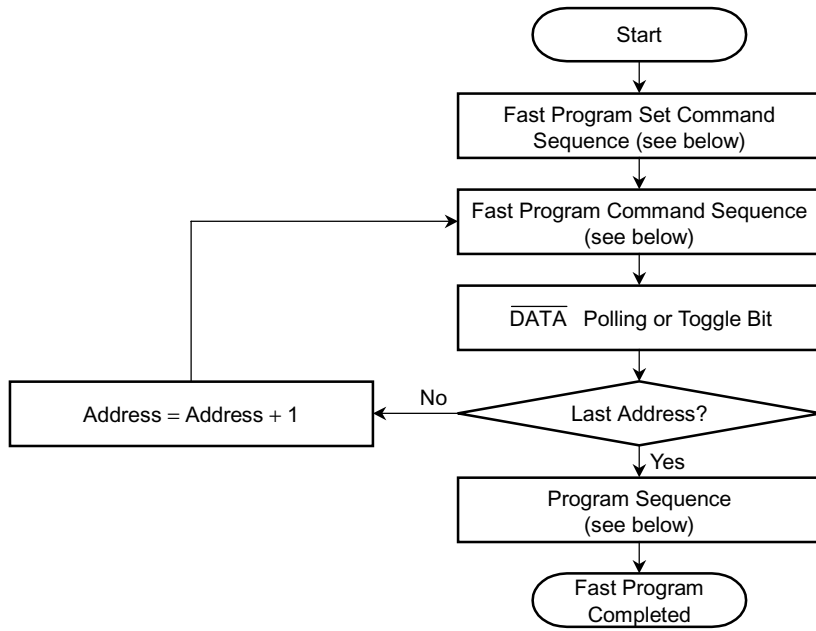


Auto-Program Command Sequence (address/data)

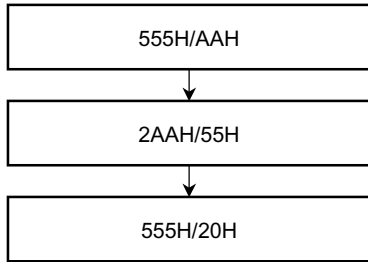


Note: The above command sequence takes place in Word Mode.

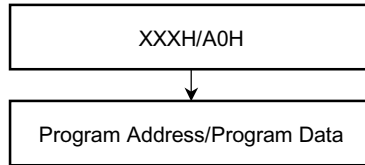
Fast Program



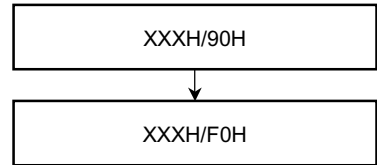
Fast Program Set Command Sequence (address/data)



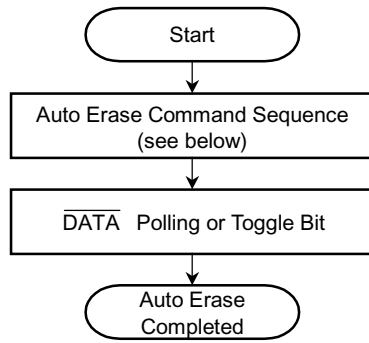
Fast Program Command Sequence (address/data)



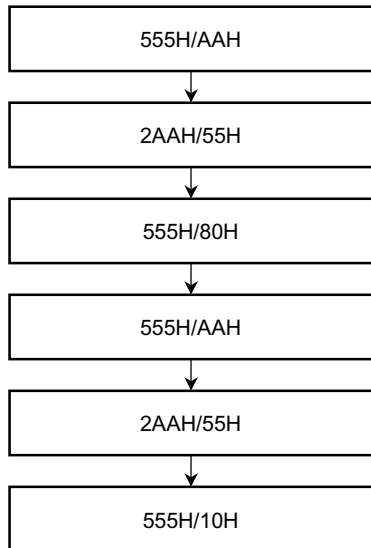
Fast Program Reset Command Sequence (address/data)



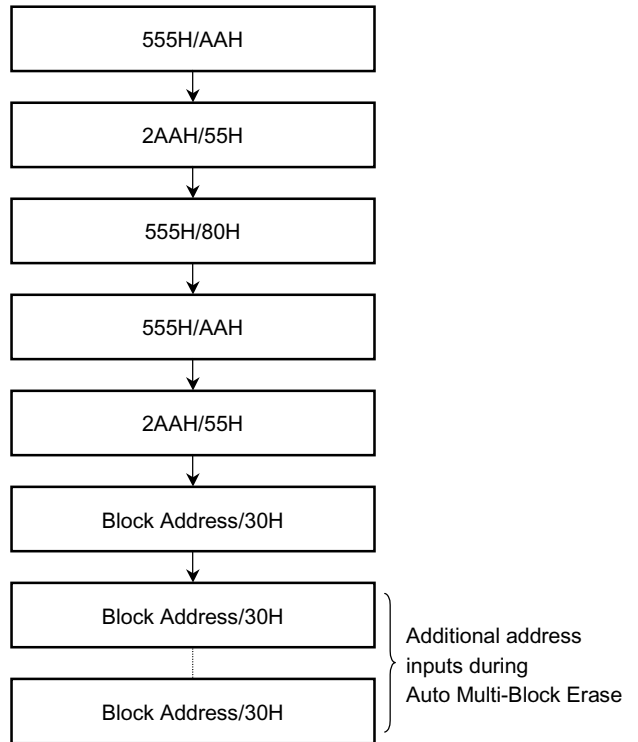
Auto Erase



Auto Chip Erase Command Sequence
(address/data)

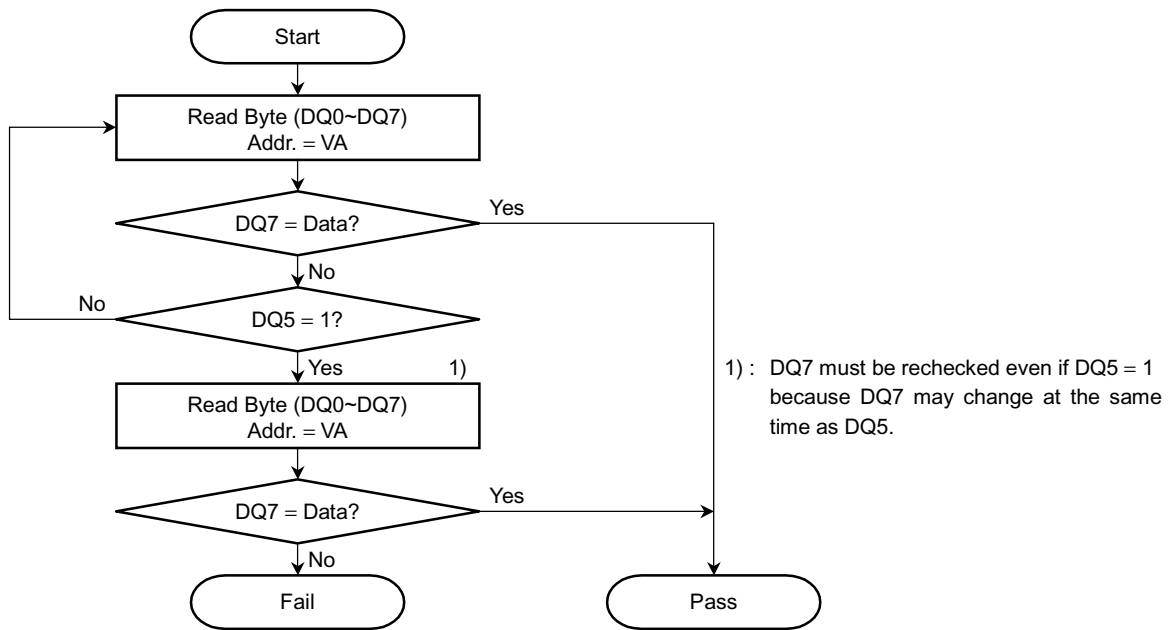


Auto Block / Auto Multi-Block Erase Command Sequence
(address/data)

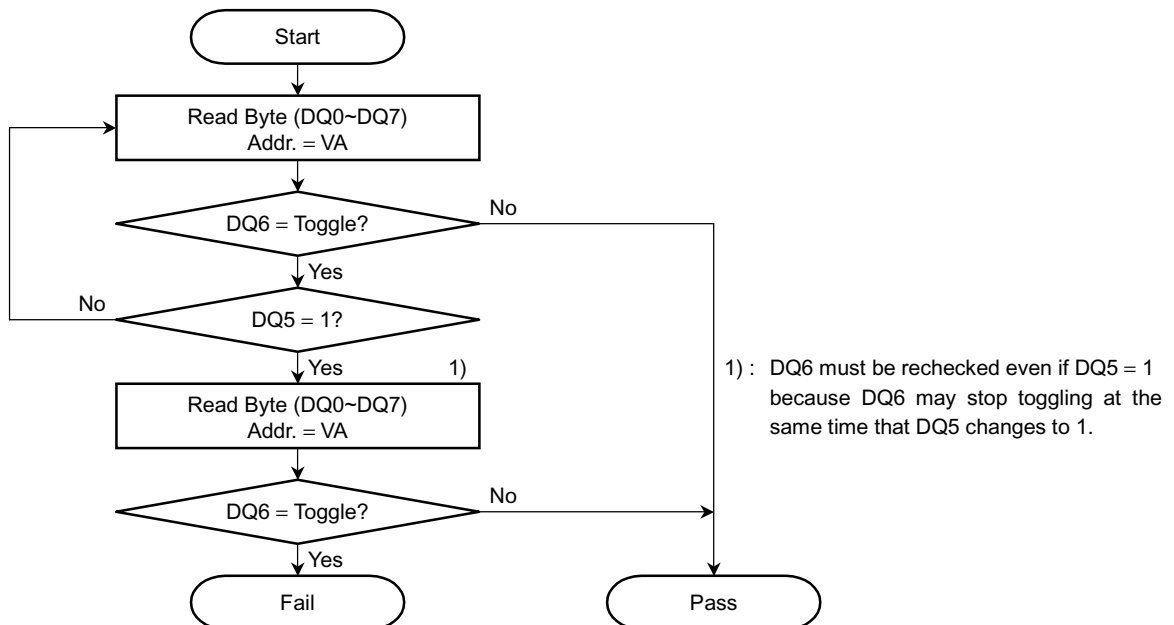


Note: The above command sequence takes place in Word Mode.

DQ7 DATA Polling



DQ6 Toggle Bit



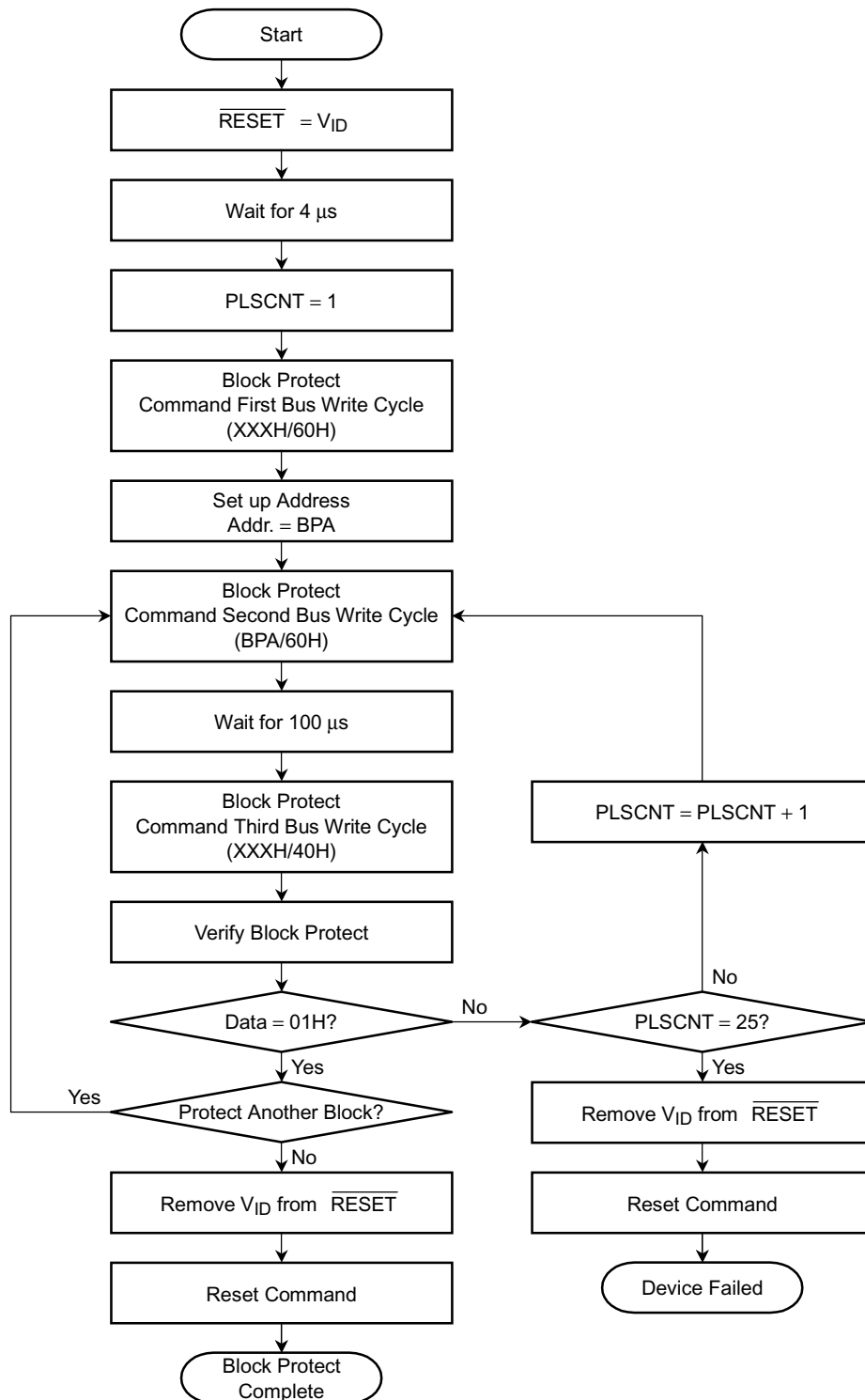
VA: Byte address for programming

Any of the addresses within the block being erased during a Block Erase operation

“Don't care” during a Chip Erase operation

Any address not within the current block during an Erase Suspend operation

Block Protect



BPA: Block Address and ID Read Address (A6, A1, A0)
 ID Read Address = (0, 1, 0)

PACKAGE DIMENSIONS

Unit: mm

P-FBGA69-1209-0.80A3

